Agilent N1225A Four-Channel High Resolution Laser Axis Board for VME

User's Guide

Agilent Technologies

Notices

Manual Part Number

N1225-90012

Edition

Second Edition, July 2007

Printed in USA

Agilent Technologies, Inc.
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Santa Clara, California 95052-8059

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User's Guide

This guide describes how to use the Agilent N1225A Four-Channel High Resolution Laser Axis Board for VME.

Agilent N1225A Four-Channel High Resolution Laser Axis Board for VME

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This product and related documentation must be reviewed for familiarization with this safety markings and instructions before operation.

Before Cleaning

Disconnect the product from operating power before cleaning.

Warning Symbols That May Be Used In This Book

Instruction manual symbol; the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual.

Indicates hazardous voltages.

Indicates earth (ground) terminal.

or

Indicates terminal is connected to chassis when such connection is not apparent.

Indicates Alternating current.

Indicates Direct current.

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An uninterruptible safety earth ground must be maintained from the mains power source to the product's ground circuitry.

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ANY INTERRUPTION OF THE PROTECTIVE GROUNDING CONDUCTOR (INSIDE OR OUTSIDE THE PRODUCT'S CIRCUITRY) OR DISCONNECTING THE PROTECTIVE EARTH TERMINAL WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY. (GROUNDING ONE CONDUCTOR OF A TWO CONDUCTOR OUTLET IS NOT SUFFICIENT PROTECTION.) WHENEVER IT IS LIKELY THAT THE PROTECTION HAS BEEN IMPAIRED, THE PRODUCT MUST BE MADE INOPERATIVE AND BE SECURED AGAINST ANY UNINTENDED OPERATION.

For additional safety and acoustic noise information, see back matter.

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Introduction

Purpose

This manual provides general information, installation information, operating information, theory of operation, exchange assembly details, manual changes, maintenance and service information for the Agilent Technologies N1225A Four-Channel High Resolution Laser Axis Board for VME.

Audience

This manual is intended for anyone who wants to design the Agilent N1225A into an OEM system, needs to supply additional capability to an existing compatible system or who needs the information in a lab environment for experimental purposes.

To use the Agilent N1225A, knowledge of how to read and write data to addresses in the VMEbus backplane is needed, along with basic programming skills. The Agilent *Laser and Optics User's Manual* describes alignment and setup of laser heads and interferometers.

Reference documentation

The following publications may be helpful companions to this manual. The first two cover VMEbus operation, and the third one covers setting up the optics used with the Agilent N1225A board. The *Laser and Optics User's Manual* is recommended as a reference for setting up your optics.

- *ANSI/VITA 1-1994 American National Standard for VME64*
- *ANSI/VITA 1-1997 American National Standard for VME64 Extensions*
- *Agilent Laser and Optics User's Manual*, part number 05517-90086 and CD part number 05517-13602 (for help selecting optical components and alignment)
- CD of *Agilent N1225A Four-Channel High Resolution Laser Axis Board for VME User's Guide*, part number N1225-13602 (this manual on CD)

Manual Conventions

Register addresses

"$" prefix: The Agilent N1225A uses "register based programming" to control the board. The register locations are specified as "offsets" from the board's base address using hexadecimal numbering (Note: hex numbers have a $ prefix). To get the absolute address, add the offset to the base address.

Numeric constants

"$" prefix: Hexadecimal constants are represented as in the Basic programming language using the prefix: "$" as in $FC01 to represent the hexadecimal equivalent of the decimal number 64513.

Word length

"Word" and "Long Word": An addressable unit of data of length. "Word" contains 16 binary bits. A "Long Word" contains 32 binary bits.

Bit positions

When a register bit position is referred to by bit number as in "bit 11 of the General Status & Control register", the implied numbering begins with bit 0 as the least significant register bit.

Low true signals

A tilde "~" as the leading character in a signal name indicates that the signal is "low true" in the conventional logic signal sense with positive true logic.

Logical conditions

"reset" means clearing a bit or setting a register to zero.

"clear" nominally means setting to zero or removing a condition, as in "clearing an error condition" and restoring the board or axis to normal operation.

"set" means setting a bit to "1" or logical "TRUE".

Latched bit

Once a latched bit is set, it remains set until specifically cleared. If the condition that caused the bit to be set is still present, the bit will be set again. Generally, writing a “1” to the latched bit will clear it. For bits that are an ORed combination of other bits, a single write to the ORed bit position will clear all of the ORed together bits.

Real-time bits and registers

Real-time means the status is constantly updated to indicate the state of the condition being monitored.

Reserved bits

These bits are not currently used. Write zeros when writing to reserved bits. Reserved bits always read zero.

Agilent N1225A Features/Capabilities

This section briefly describes the capabilities of the Agilent N1225A Four-Channel High Resolution Laser Axis Board for VME, points out the functional differences from the Agilent 10897A/B/C and Agilent 10898A boards (referred to as "10897/8" boards in this manual) and identifies basic retrofitting issues. Subsequent chapters provide detailed descriptions of the operation, programming, and hardware interface to the Agilent N1225A.

Capabilities

The N1225A axis board is a VME64x "6U" size board with four optical channels that can support a three-axis laser measuring system, where one channel, channel four, is used for the optical reference and the other three channels receive light from the measurement axes. For greater numbers of axes, a laser reference derived from channel four is passed between boards using Agilent supplied Reference Passing patch cables. The maximum number of boards in the reference chain is eight.

The N1225A is designed for use in VME64x backplanes and can be used, with some limitations, with 10897/8 boards in the same backplane. It has five row connectors but can operate in a three row connector backplane environment to maintain compatibility with the 10897/8 boards, providing most of their functions. The P2 connector rows, A and C, have pin-for-pin compatibility with the 10898A, and limited* compatibility with the 10897. Extra features of the N1225A are accessible over the P2-D and -Z rows.

NOTE **A 5-row connector backplane is not required to use the N1225A. The behavior of P2 rows A and C of the N1225A matches the 10898A. When replacing the 10898A with the N1225A, software changes and installation of an optical reference are required.**

* Incompatibilities with the 10897x: The N1225A does not support the input of reference and measure signals at pins P2-A1 and P2-A2. These pins are used for addressing the board or the P2 signed magnitude position output. Data age is also different. It does not support the **window out** signal at pin P2-A5 or the clip mask function. Other incompatibilities are covered in the following pages and in Chapter 3, "Operating the Agilent N1225A.

Features

- Plane mirror resolution of 0.15nm
- Range = 20.6m or ±10.3m
- Velocity limits: ±2.29 m/s with 15 MHz laser split frequency; ±0.87 m/s for 6 MHz
- Maximum axis acceleration: 400g
- High sensitivity on-board receivers with ST connectors
- Less slots needed in VME rack. A single board accommodates 3 axes of motion; for two boards, 7 axes; 3 boards, 11 axes ...
- Reference signal can be daisy chained between multiple N1225A boards
- New algorithm has higher immunity to “glitches”
- High speed parallel outputs provide four axes of simultaneous position at 10 MHz (10 bits/axis—this limits the velocity that can be followed to less than 768mm/s when using plane mirror optics)
- P2 A&C row position and control I/O backward compatible with Agilent 10898A board, and in many applications with 10897A,B,C boards
- A16/A24/GAP addressing, D16/D32 data transfers, interrupts
- Single power supply: +5V, 5.6A maximum
- 10/100 BaseT LAN, DHCP enabled, imbedded web page server, access to most registers through web page for viewing and modification
- “Trace” capability
- Self test capability
- Two velocity and position comparators per axis with external hardware output
- Absolute phase available
- Can lock to external 10 MHz clock supplied over backplane

Agilent N1225A Front Panel

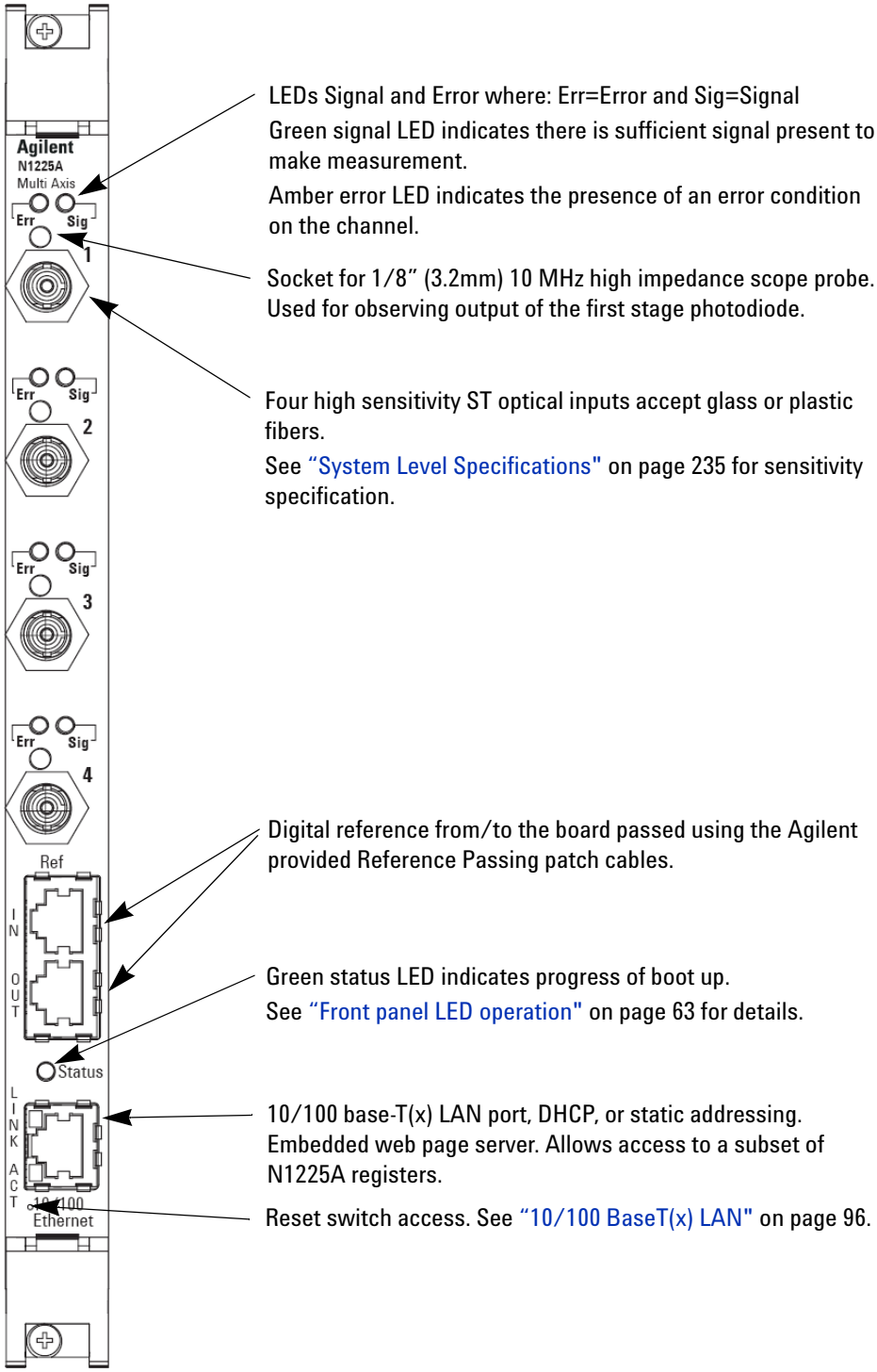


Figure 1 Agilent N1225A front panel

Agilent N1225A Side View

S1: Used to set the bus address bits, A18–A11. See Chapter 3.

S2: Used to select A24/A16/GAP addressing and address bit A23–A19. See Chapter 3.

S3: Factory use only.

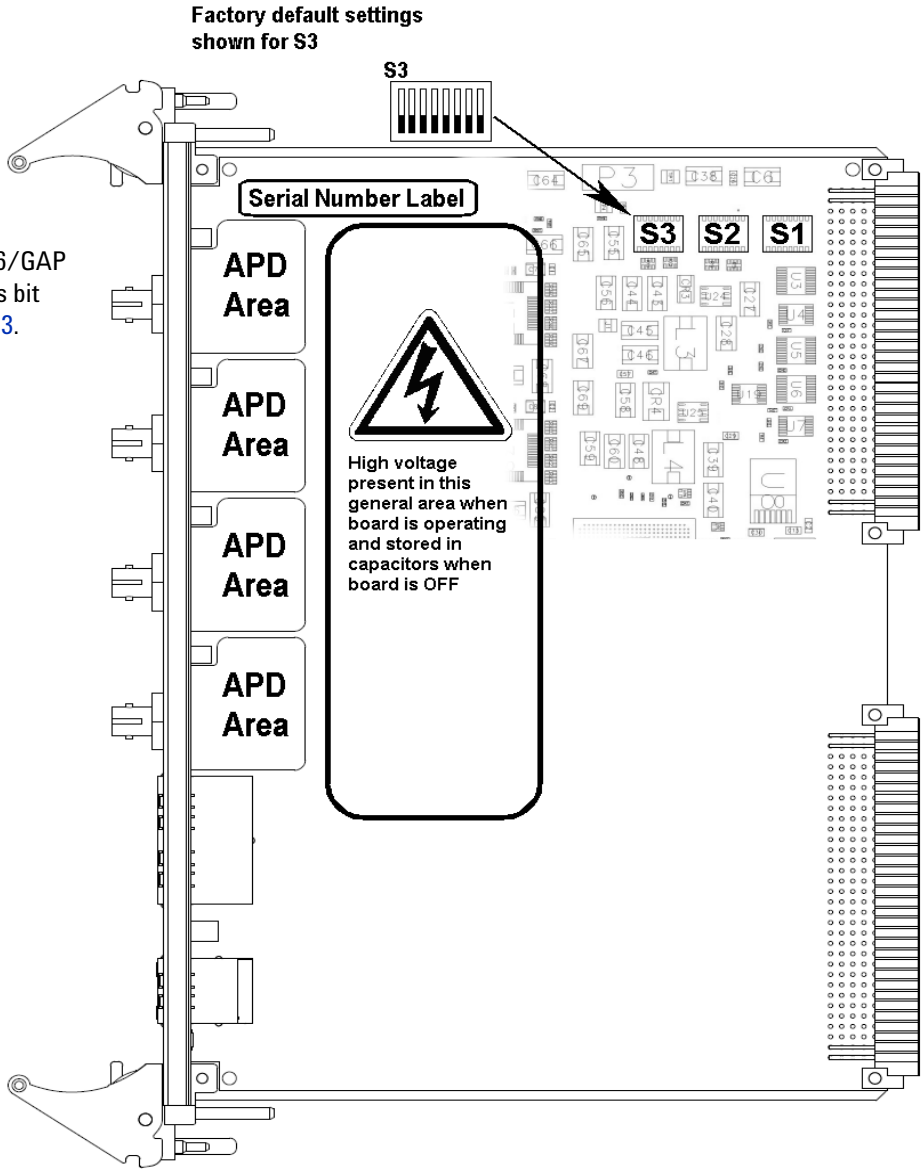


Figure 2 N1225A side view

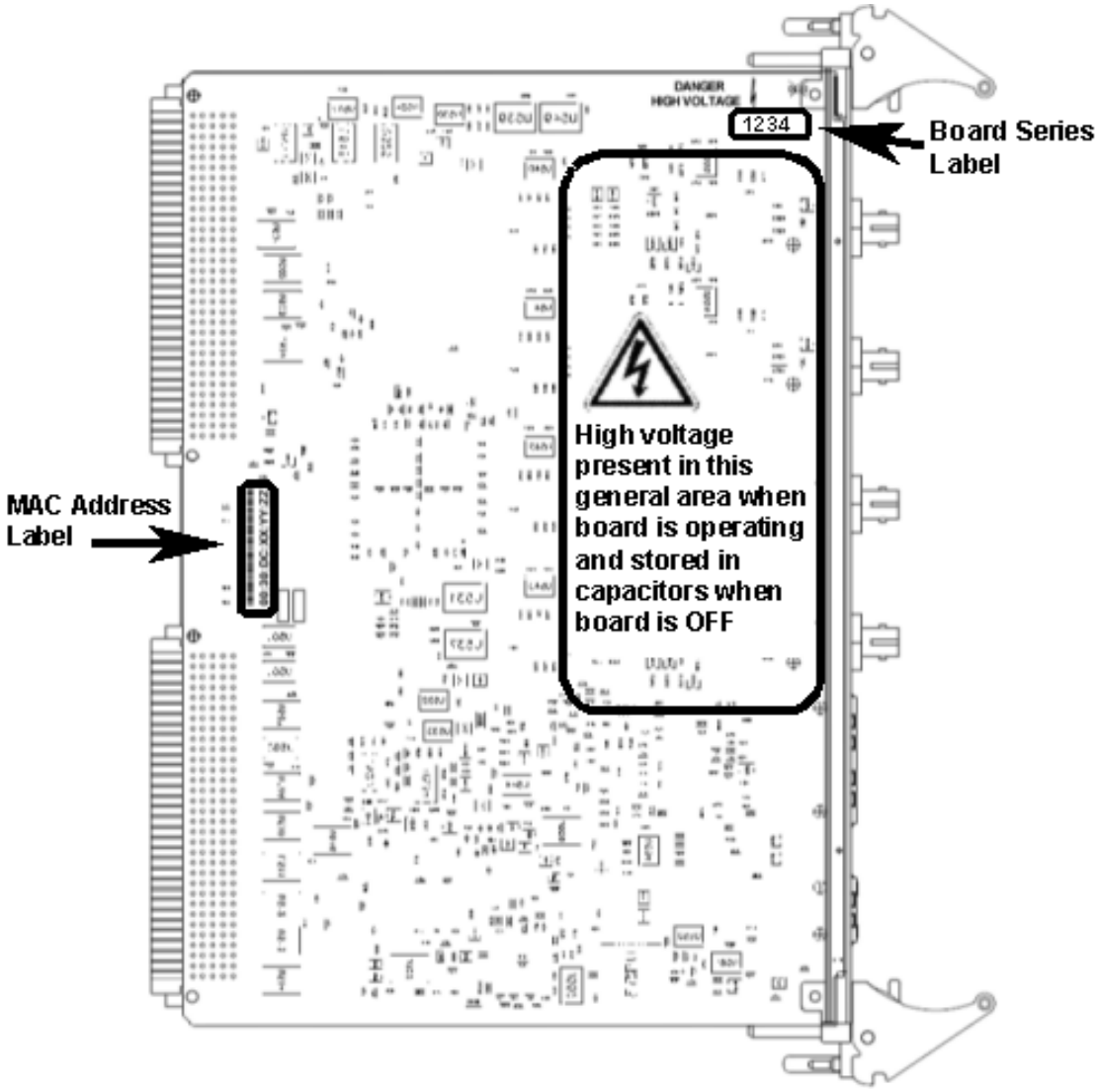


Figure 3 N1225A circuit side view

Example

Figure 4 shows the N1225A used to measure stage position with three interferometers. In this figure the X, Y, and stage rotation are measured and the position is output over the A and C rows of P2 directly to customer supplied hardware. The VME controller sets up the laser axis board to make the measurements.

NOTE The optical reference goes to channel 4 of the laser axis board.

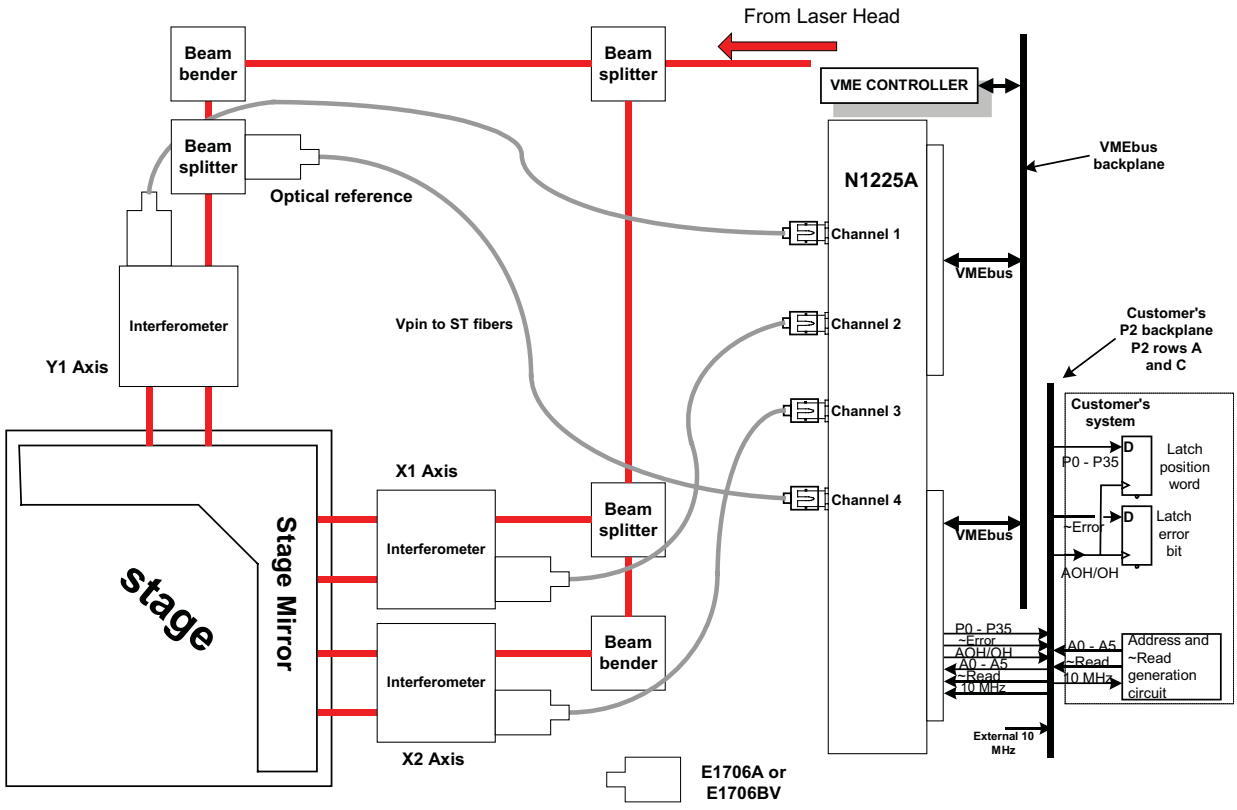


Figure 4 Three-axis optics and N1225A

Comparing the N1225A, 10898A, and 10897A/B/C Boards

Compatibility with the 10898A and 10897A/B/C boards

- The N1225A P2 bus I/O is designed to be compatible with the 10897/8 boards but not all features are supported. The key differences are identified in Table 1.
- Like the 10897/8 boards, unaligned bus transfers over the VME bus are not supported. Thirty-two bit reads/writes can only be made from addresses evenly divisible by four, and 16 bit reads/writes must be made using even addresses.
- Unlike the 10897/88 boards, the N1225A requires only a +5 V power supply.

Incompatibilities with the 10897/10898 boards

- The N1225A cannot accept reference signals coming from laser heads or the replicated reference signal coming from 10897/8 boards. Nor can it output a reference signal compatible with the 10897/8 boards. Single board systems require an optical reference, and boards in multiple board systems use a reference passed from the adjacent board.
- The N1225A supports 10897/8 Asynchronous Modes 0, 1, 2 and 3.
- For software compatibility, the N1225A register map is based on the 10897/8 maps, but modifications to existing software functions and addition of new routines is needed to manipulate the appropriate bits. The N1225A and 10897/8 register structures are similar to reduce the effort required to leverage existing software (and hardware).
- Addressing: In the VME address map, many compatible registers are in the same location as on the 10897/8 boards, with added registers at new locations. N1225A base addresses for axes match 10897/8 boards but with larger spacing between board addresses for multiple board systems. For example, if board0 base address is at $000000, the board1 base address would be at $000800, board2 at $001000 and so forth. Address offset for axes match the 10897/98 boards. For example, if axis0 address offset at $000000, then axis1 offset is $000200, axis2 offset = $000400, axis3 offset = $000600. A16 and A24 addressing is supported.

A summary of the major differences between the N1225A and 10897/8 boards is shown in Table 1.

Table 1 Major Similarities and Differences Between N1225A and 10898A P2 Bus Behaviors

Attribute	10897/8	N1225A
P2 position word	36 bit P2 position	Same
Maximum data rate	10 MHz/# of axes	10 MHz/# of axes for P2 rows A&C, 10 MHz per axis outputs on rows D&Z
Synchronize all boards in backplane to 10 MHz clock	Yes	Yes, the first board is synchronized to the backplane 10 MHz and remaining boards are synchronized using signals on the reference passing cable.
Async mode 0	Yes	Yes, but now four axes are affected instead of 2.
Async mode 1	Yes	Yes, but now four axes are affected instead of 2.
Async mode 2	Yes	Yes
Async mode 3	Yes	Same
Address lines A0-A5, ~Read line	Yes	Same
~Position reset line	Yes, affects 1 or 2 axes	Yes, affects 4 axes
~Force zero line	Yes, affects 1 or 2 axes	Yes, affects 4 axes
~Sample1 thru ~Sample4 lines	Yes	Same
Output Hold line	Yes, affects 1 or 2 axes	Yes, affects 4 axes
P2 Signal Timing	Defined in Chapter 8	Compatible
Ref and Meas inputs on P2	Supported on the 10897, not supported on the 10898	Not supported
Window output	Supported on the 10897, not supported on the 10898	Not supported at P2-A5. Can be implemented using comparators.
Clip mask	Yes	Not supported
P2 signed magnitude output format	Yes	Not supported
One N1225A board can be used in place of two Agilent 10898A boards when reference passing from another board is used.		

Using the N1225A in Place of a 10898A Board

If the current system takes data from the 10898A or 10897A,B,C P2 A&C rows, the N1225A is designed for backward compatibility with these boards. Here are items to consider when designing the N1225A into these types of systems. More information can be found in Chapter 3, “Operating the Agilent N1225A”.

- The N1225A needs an optical reference, which is a portion of the incident laser beam.
- Current draw is 5.6A maximum on +5V vs. 4.5A maximum for the 10898A.
- Although the N1225A has five row connectors, it works in the three row backplane to maintain compatibility with the 10897/8 boards.
- Fibers with ST connectors are needed to bring light from the interferometers and optical reference to the board. Agilent offers the E1705B series (plastic Vpin to ST), E1705E series (glass Vpin to ST) and E1705F series (glass ST to ST) fibers in various lengths.
- 10 MHz backplane clock frequency tolerance is more stringent, it is 10 MHz ±100 ppm.
- The N1225A does not have the clip-mask function or P2 signed magnitude output format or window output.
- Most registers are in similar locations in the address maps, but software functions will need to be changed to match the N1225A register map.
- Data age is different for the N1225A.
- The N1225A does not have a Position Offset Register for use in creating the P2 position output value. The Position Offset-Sign Extend register is also not present in the N1225A.

2
Installing the Agilent N1225A

Introduction

This chapter contains important setup information that applies to all VMEbus applications in which the Agilent N1225A is used. It also provides a few practical suggestions that will make installation and operation of the Agilent N1225A easy and reliable.

Options

Table 2 Options

Item	Option Number
Reference cable	N1225A-002
Manual on CDROM	N1225A-101

Additional parts needed

Fiber optic cables

If you are replacing 10897/8 axis board(s) with the N1225A, the fiber optic cables may need to be replaced with cables that have ST connectors. Refer to these Agilent product numbers:

- Agilent E1705B-XXX Plastic Vpin to ST fiber
- Agilent E1705C-XXX Plastic ST to ST fiber
- Agilent E1705E-XXX Glass Vpin to ST fiber
- Agilent E1705F-XXX Glass ST to ST fiber

Where XXX is the option number of the product and designates the nominal fiber length.

Table 3 lists the standard fiber lengths available.

Table 3 Standard fiber cable lengths

Option (XXX)	Fiber Length
004	0.2 m +5 mm –0 mm
020	1 m +10 mm –0 mm
025	1.25 m +10 mm –0 mm
040	2 m +20 mm –0 mm
050	2.5 m +20 mm –0 mm
060	3 m +20 mm –0 mm
080	4 m +20 mm –0 mm
100	5 m +20 mm –0 mm
120	6 m +20 mm –0 mm
140	7 m +20 mm –0mm
160	8 m +20 mm –0 mm
180	9 m +100 mm –0 mm
200	10 m +100 mm –0 mm

Laser head cables

Table 4 lists the laser head cables with no reference leg, that carry power only. They are available under the part numbers listed in the table. The cables are shown in figures 5 thru 7.

Table 4 Power only laser head cables

Part Number	Description
E1847A-060	Laser Head Power only cable, 3 m +0.15 m, –0 m; #6 spade lugs
E1847A-140	Laser Head Power only cable, 7 m +0.15 m, –0 m; #6 spade lugs
E1847A-200	Laser Head Power only cable, 10 m +0.15 m, –0 m; #6 spade lugs
E1847A-300	Laser Head Power only cable, 15 m +0.25 m, –0 m; #6 spade lugs
E1847A-400	Laser Head Power only cable, 20 m +0.25 m, –0 m; #6 spade lugs
E1848A-060	Laser Head Power only cable, 3 m +0.15 m, –0 m male DIN connector
E1848A-140	Laser Head Power only cable, 7 m +0.15 m, –0 m male DIN connector
E1848A-200	Laser Head Power only cable, 10 m +0.25 m, –0 m male DIN connector
E1848A-300	Laser Head Power only cable, 15 m +0.1 m, –0 m male DIN connector
E1848A-400	Laser Head Power only cable, 20 m +0.25 m, –0 m male DIN connector
E1848B-060	Laser Head Power only cable, 3 m +0.15 m, –0 m; female DIN connector
E1848B-140	Laser Head Power only cable, 7 m +0.15 m, –0 m; female DIN connector
E1848B-200	Laser Head Power only cable, 10 m +0.15 m, –0 m; female DIN connector
E1848B-300	Laser Head Power only cable, 15 m +0.25 m, –0 m; female DIN connector
E1848B-400	Laser Head Power only cable, 20 m +0.25 m, –0 m; female DIN connector

Figure 5 E1847A Laser head connector to #6 spade lugs

Figure 6 E1848A Laser head connector to 5-pin male DIN

Figure 7 E1848B Laser head connector to 5-pin female DIN connector

Power and Environmental Considerations

The Agilent N1225A is a high speed VMEbus card that takes maximum advantage of VMEbus capabilities. For this reason, it is critical to keep the laser axis board working within the well-defined electrical and physical environments provided by the VMEbus specification and this manual. Standard off-the-shelf VMEbus enclosures and backplanes commonly provide adequate support when they are properly set up. If you are using the laser axis board in a custom enclosure, be sure to comply with all environmental constraints specified in this manual and in the latest Agilent service notes for the N1225A. Service note information is available at Agilent.com. The critical areas are discussed in the following sections.

- Working voltage
- Cooling
- P2 connector compatibility

Working voltage

The laser axis board draws a maximum of 5.6 A from the +5 V VMEbus power supply. At a current level this high, it is easy to accumulate unexpected voltage drops that can result in a lower than expected supply voltage at the laser axis board. For example, simply putting the laser axis board on an extender card can reduce the supply voltage enough for the resulting voltage to be out of the VMEbus specification range of 5 V +0.25 V, –0.125 V.

NOTE The voltage at the backplane connector that the board is plugged into must be within the specified limits under worst case conditions of the current draw.

The low supply voltage is an absolute limit. As per the VMEbus specification, the laser axis board is designed to be operated at a minimum absolute voltage of +4.875 V on the +5 V rail. If the operating voltage is allowed to fall as low as +4.75 V some of the internal circuits, for example the P2 bus drivers, will be disconnected and operation of the P2 bus will essentially shut down. This will not harm the laser axis board but it will interrupt system operation if the P2 Hardware Position output is being used.

NOTE

The specified VMEbus voltage range is not symmetric around +5 V. Unfortunately, this is not usually noticed and there is a tendency to set the +5 V supply voltage to exactly +5.0 V, especially on purchased VMEbus enclosures. This provides very little margin for the unavoidable small voltage drops that always seem to occur.

Recommendation: Set the +5 V rail voltage of the VME enclosure to 5.20 V, which is close to the VMEbus specification maximum of +5.25 V.

Operating temperature and cooling

The N1225A total power dissipation is about 25W. Since it is not uncommon to operate ten or more VMEbus boards in the same enclosure, the total power dissipation in a relatively compact space can easily exceed 250W and can easily cause board temperature limits to be exceeded.

CAUTION

A cooling system failure or inadequate air flow could have serious consequences, including intermittent errors. To prevent board damage, the high voltage supply will be turned off if the temperature in the optical receiver section reaches 60° C. This will stop the measurement process and set an error bit.

With regard to cooling, the laser axis board is most reliable when operated within the specification range (see "Operating environment" on page 236). The penalty of operating outside of this range is reduced reliability (failure rates are generally assumed to double every 10° C). It is not possible to guarantee the system performance outside of the specified ranges for temperature, voltage, and air flow.

Usually, the question of whether the laser axis board is being adequately cooled arises when custom enclosures are being considered. Although the VMEbus specification defines air flow rates, the real issue is temperature rise above ambient on the surfaces of components and boards. High air-flow rates are specified in order to keep these temperature rises reasonably low.

Recommendation: At all times when power is applied, you should provide sufficient air flow to keep the temperature of the APDs, located in the receiver section, below 60° C. See Figure 2 on page 22.

Installation

Figure 8 shows a simple single board system configuration that provides an example of how the N1225A would be connected to a measurement laser. The only special precaution to follow when connecting the cables is to make sure you do not exceed the minimum bend radius of the optical fiber cables. Bending them beyond this minimum will decrease their efficiency and increase the optical power needed to make a measurement.

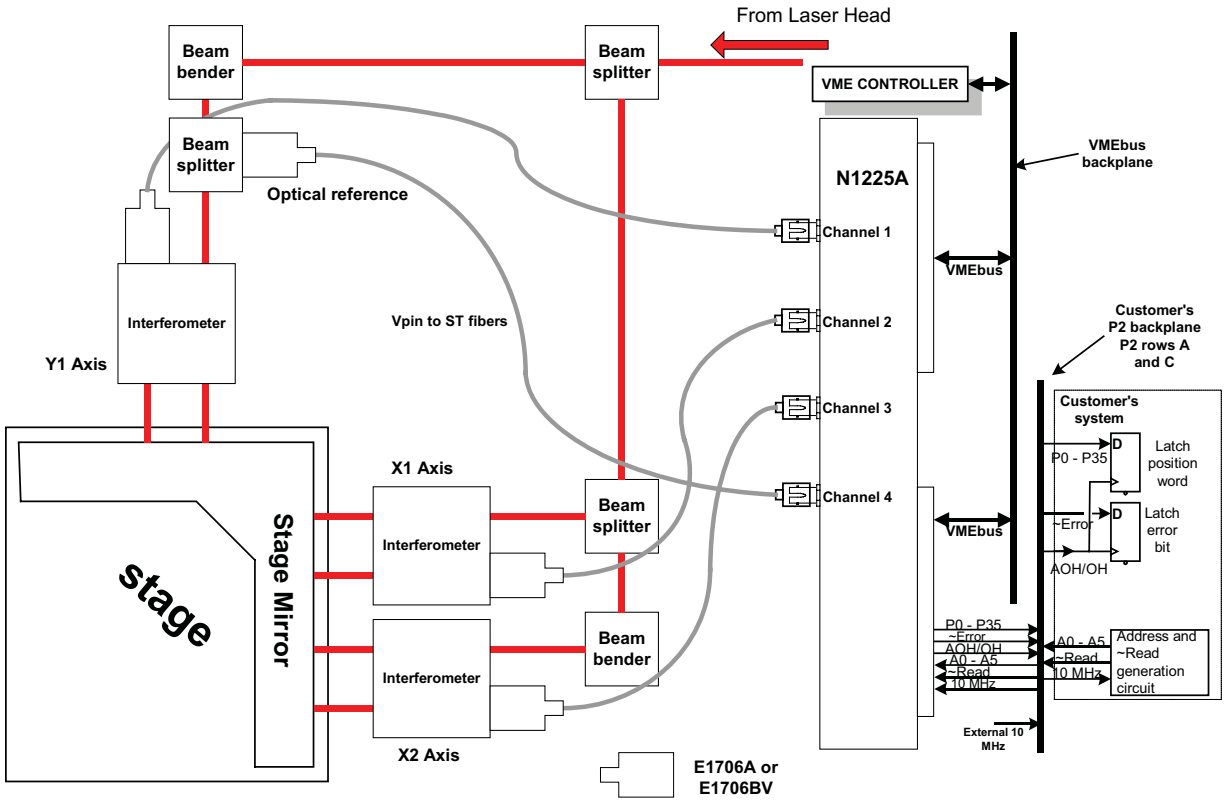


Figure 8 Typical cable configuration

Installing the Board

Overview

To install the laser axis board you will:

- Verify switch S3 is in the factory default position.
- Set the board address.
- Place the boards in rack.
- Install the reference cables.
- Connect fibers to channels 1 through 4 of the boards.

Procedure

1 Refer to Figure 2 on page 22. Verify all individual switches in S3 are down, as shown.

2 Set the VMEbus address.

Each laser axis board requires a unique address in the VMEbus address space. Typically, multiple boards are assigned consecutively higher addresses. The base address of each board is assigned by setting the S1 and S2 dip switches on the laser axis board to the high-order bits of the binary representation of the required VMEbus address starting with bit A11. Consider bits A10 through A0 as set to zero for purposes of setting the base address.

There are four modes for addressing the N1225A board.

- A16
- A24
- A16 plus GAP (Geographical Addressing Protocol)
- A24 plus GAP

In A16 and A24 mode, the base address is set using S1 and S2, with the mode specified using the A16/A24 switch on S2. When GAP is selected, bits A15 through A11 of S1 are replaced by GAP values from the five row VME64x backplane.

The function of each switch position, and some sample address settings are shown in figures 9 through 11.

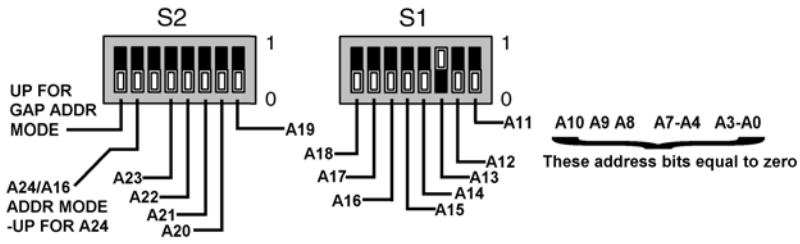


Figure 9 Function of each switch position

Figure 10 Address switches set for A24 mode, Base address (hex) = $183800

Figure 11 Address switches set to A16 mode, base address (hex) = $C800

Address switch positions A23 through A16 are ignored when using A16 addressing.

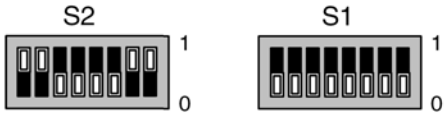


Figure 12 Address switches set to A24 GAP addressing mode

Higher order bits, A23 through A16, are set using S2 and S1 while lower order bits, A15 through A11 are determined by GAP. Bits A10 through A0 equal zero, as before. This works similarly in A16 GAP addressing mode.

3 Place the board in the rack.

To accommodate the reference cable, place boards adjacent to each other or have no more than one slot between them.

4 To install the reference cable, locate the N1225A that will receive the optical reference signal.

5 Plug one end of the reference cable into the RJ-45 connector labeled OUT.

CAUTION Do not plug the reference cable into the 10/100 Ethernet port.

6 Plug the other end of the reference cable into the reference IN connector of the next board.

7 Continue installing the rest of the reference cables, going from the reference OUT connector of one board to the reference IN connector of the next board until all boards are chained together.

8 Complete the installation by connecting the fibers from your system to channels 1 through 4 of the laser axis boards.

Power Up and Verification Procedure

This procedure is for checking the board when you receive it from Agilent. It assumes the N1225A is in its “as shipped” condition with the LAN setting DHCP enabled. If the board is not in its “as shipped” state, please stop here and use the verification procedure in the Maintenance chapter instead of this one.

Equipment list

- VME 6U size rack with P1 and P2 connectors and capable of providing +5V at 5.6A.
- 10/100 BaseT router or switch capable of assigning IP addresses via DHCP enabled Ethernet boards or an available LAN port on a network which supports DHCP.
- LAN patch cable to connect the laser axis board to a router or network connection. When connecting to your network or to a router, the standard straight-through patch cable is normally used.
- Networked computer with web browsing capability attached to either the workspace network or the router.

Setup

Before plugging the board into the VME cage, some information needs to be copied from the board labels.

1 Write down the board serial number, which is located on the top side of the board in the upper left corner. The serial number format is “US00000000”. See Figure 2 on page 22 for label location.

2 Turn the board over and find the MAC address label, located near the P1 and P2 160-pin connectors and write down the MAC address, which is in the form “00:30:DC:09:48:21” See Figure 3 on page 23 for label location.

3 Verify the VME rack power is turned OFF.

The N1225A does not support hot-swapping.

4 Insert the laser axis board into any available slot.

5 Connect the LAN cable to the laser axis board 10/100 Ethernet port.

NOTE Be careful not to plug the LAN cable into the reference in/out connectors.

Perform the Power Up Procedure

1 Turn on the router or switch.

2 Turn on the computer being used.

3 Locate the Status LED on the laser axis board front-panel because it indicates board boot-up progress during the next step in this procedure.

4 Turn on the VME rack and observe the laser axis board status LED.

a Status LED begins flashing green after the VME rack +5V is supplied to the board.

b Status LED continues to flash for 15 to 30 seconds then turns on continuously green indicating the boot up process and internal self-checks have successfully completed. If this does *not* occur, stop, turn off the VME rack, and refer to Chapter 7, “Maintenance and Service.”

After boot-up completes, the board is ready to respond over the VMEbus and LAN port.

5 Start the web browser on your computer.

Use one of the following methods to obtain the DHCP assigned IP address for the board:

- If you already know the assigned IP address, then proceed to the next step. (For example, if you know the address or limited range of addresses your router or switch is setup to assign, then you can try the addresses in the web browser.)
- Open a command window or the equivalent on your computer and type `ping <hostname>` where hostname is a combination of product name and the last seven digits of the serial number, for example typing `ping an1225a-6061234`. If your DNS server supports lookup, it will return the IP address for the board. Then proceed to the next step. (If this does not work, your DNS server may not support lookup or is down.)

NOTE

It may be necessary to append domain information when pinging the board. If your board is not recognized, ping using the format:

`ping an1225a-`*`6061234.eed.mycompany.com`*, where:

6061234 = the last seven digits of the N1225A serial number
eed.mycompany.com = your domain

- Use the web browser on your computer to access the web page for the router or switch, then navigate to the appropriate page to find what IP address was assigned to the port connected to the N1225A. Proceed to the next step.
- Last, for non-PC based systems try a reverse arp lookup by typing `arp -r` followed by the MAC address for the board. This method works where there is no DNS server, but there is a DHCP server. Utilities for the PC may be available to perform this function.

6 After determining the IP address, open the web browser on the computer and enter the IP address after http://, for example, `http://130.27.43.1`. Press Enter. The N1225A Welcome page will open.

7 Check that all six fields are filled in on the Welcome page.

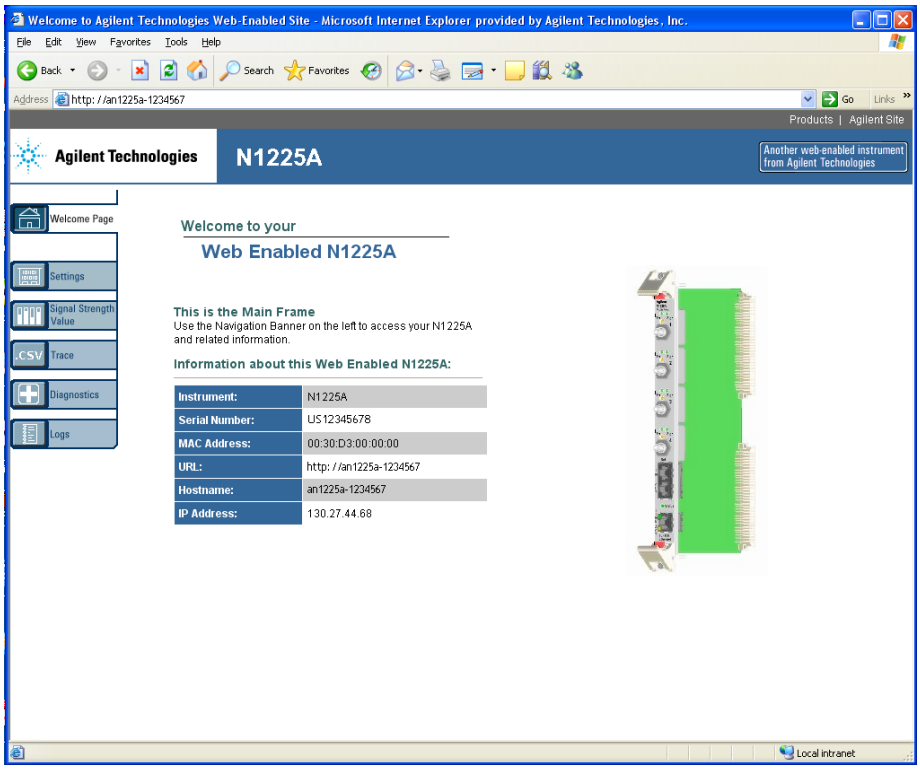


Figure 13 The Welcome window

The Settings Window

To open the Setting window, click on the Settings tab.

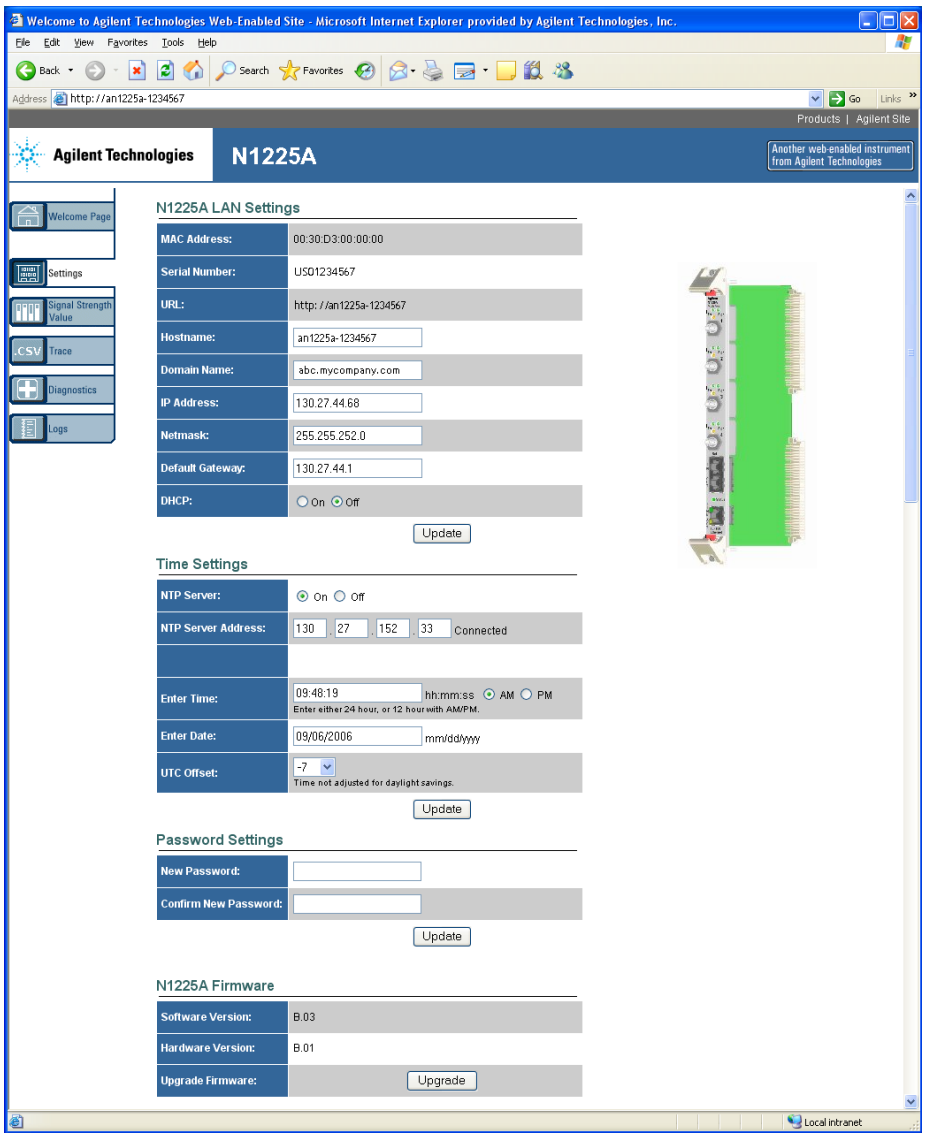


Figure 14 The Settings window

The settings page is divided into four sections.

- N1225A LAN settings
- Time settings
- Password settings
- N1225A firmware

Enter the N1225A LAN settings

The LAN Setting section of the Settings window includes the following fields.

MAC Address: This 12 character value matches the MAC address label on the circuit side of the board. See Figure 3 on page 23. It is factory set, unique to this board, and stored in the MAC address register.

Serial Number: The serial number matches the board serial number label on the component side of the board. See Figure 2 on page 22.

URL: The URL matches the URL in the address field of your web browser.

Hostname: For a newly powered up board, the factory default value: "`an1225a-1234567`" where 1234567 represent the last seven digits of the board serial number is displayed. This is read from the Hostname register and can be changed via this screen.

Domain name: The domain to which your board is connected. For example, *mycompany.com*.

IP Address: When DHCP is enabled, the DHCP server provides this value which also appears in the IP address register.

Netmask: The value retrieved from your DHCP server.

Default Gateway: Assigned by the server when DHCP is enabled.

DHCP: The factory default is ON. To change to Static IP addressing, set DHCP to OFF, enter values for the IP address and Default Gateway[optional], then click the *Update* button located below the N1225A LAN Settings section. Reestablish connection to the board by entering the IP address in your browser. When powered off, the N1225A retains the IP address and DHCP setting.

Enter the time settings

The Time Setting section of the Settings window includes the following fields.

NTP Server: Select yes or no. The default is no.

NTP Server address: If using NTP, enter the server address.

Enter time: If NTP is not being used, enter a time value here. The time value is used to time stamp the trace data file.

Enter date: Enter a date. The date is used to time stamp your trace data file.

UTC (Coordinated Universal Time) Offset: If using NTP, select your time zone using the drop down menu.

Update **button:** If any changes were made to the Time Settings section, click the *Update* button to store them.

Enter a password

Passwords: The default is no password. To require a password be entered before changing board settings, enter the password in both fields and click the Update button.

NOTE

If you are prompted to enter a user name and password, which can occur after using the RESET button to restore the board to factory default conditions, the defaults are:

User name: N1225A

Password: N1225A

View the N1225A firmware version

The N1225A Firmware section of the Settings window includes the following fields.

Software version: The version number of the software/firmware installed in this board. This information is also stored in the Board Level Firmware Revision register.

Hardware version: Reflects hardware version for board.

Upgrade Firmware button: Clicking this button opens a window which allows a new version of firmware to be downloaded to the board. Prior versions can also be loaded. See Chapter 7, “Maintenance and Service” for step by step instructions.

The Signal Strength Value Window

Click on the Signal Strength Value tab to display the Channel 1 through Channel 4 optical power levels.

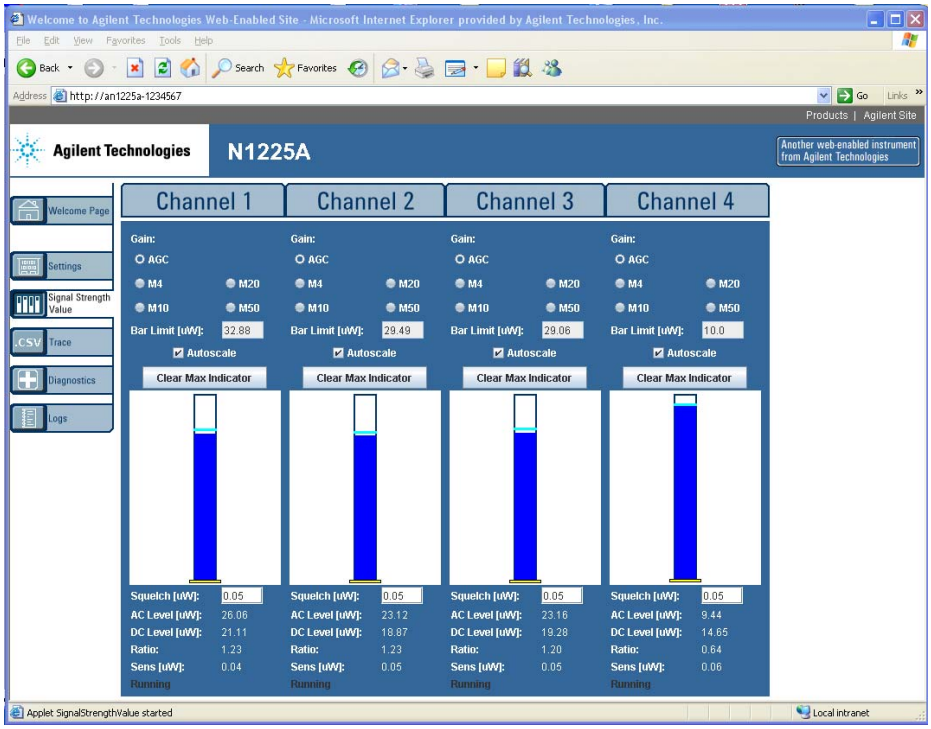


Figure 15 The Signal Strength Value window

Above the bar graph is the Gain section. By default, AGC (Automatic Gain Control) is on.

Selecting AGC off allows setting one of four fixed gain values, with M4 being the minimum gain.

NOTE Gain values and displayed power levels are not tightly calibrated and should be used for indication only.

The auto-scalable bar graph displays AC optical power level. When auto-scale is on, the bar graph range is set based on the highest power level measured. A blue bar within the graph indicates the maximum power level measured since the last time anyone clicked the Clear Max Level button. A yellow bar, which overhangs each graph indicates the squelch level. Set the squelch level by clicking and dragging the bar, or entering a value in the space below the graph.

Below the graph are the measured values.

The Trace Window

Click the Trace tab to open this window. Trace allows you to set a trigger and record position data. The section titled "The Trace Function" on page 83 describes the use of Trace.

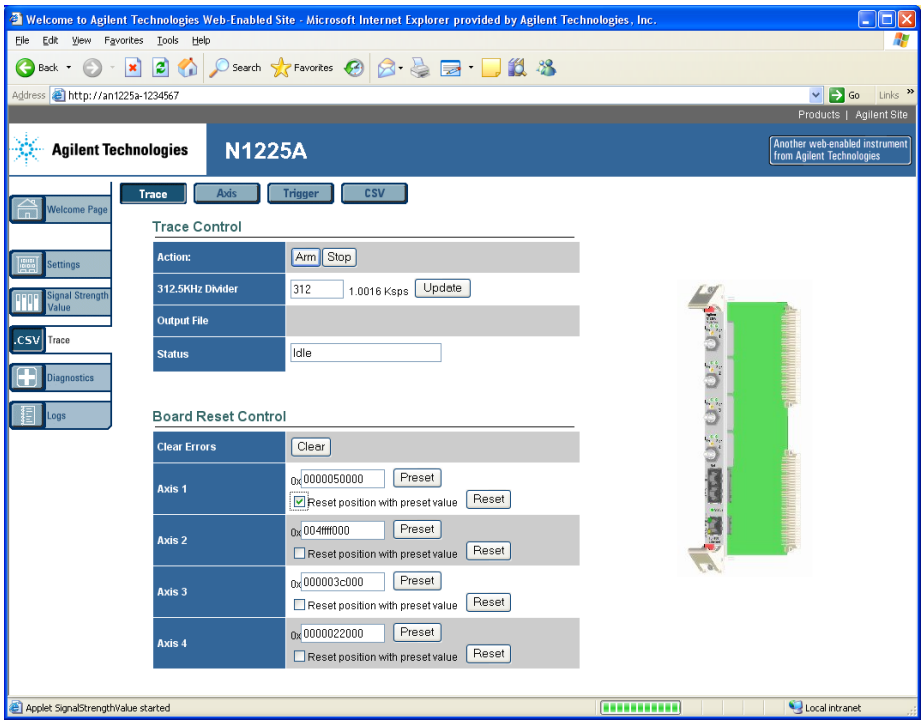


Figure 16 The Trace window

The Diagnostics Window

In Service Diagnostics Tests

Open the Diagnostics window by clicking the Diagnostics tab.

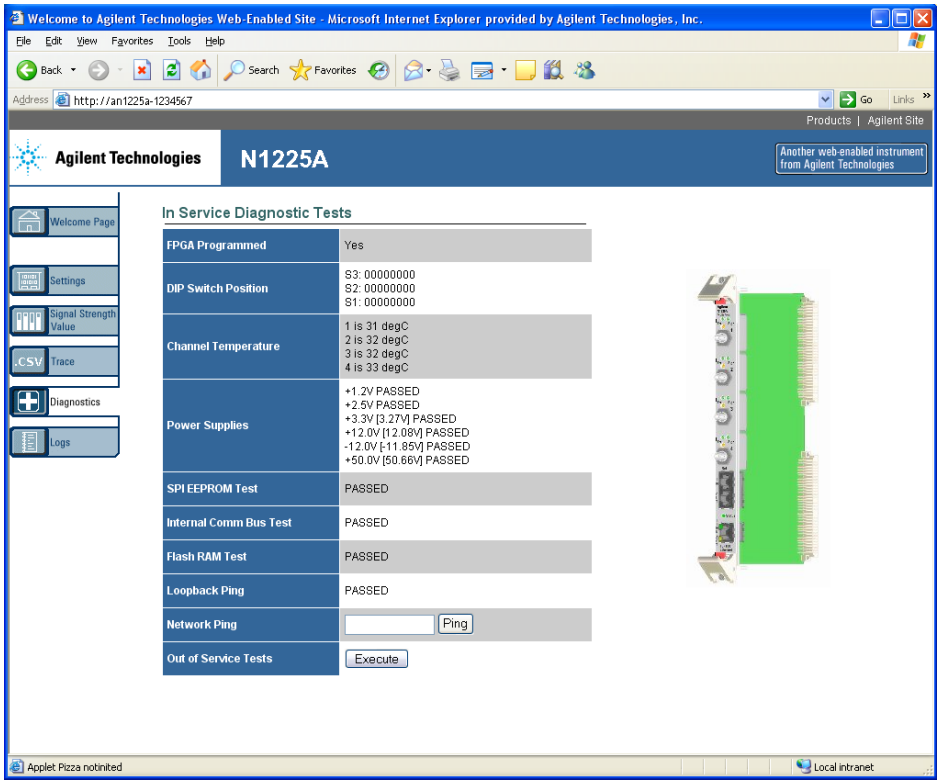


Figure 17 The Diagnostics window

Check the fields for the following values:

FPGA Programmed: Yes.

DIP Switches: S3 should be all zeros. S2 and S3 are used for setting the board address and should reflect the current switch position. A zero means the switch is in the down position relative to the orientation of text on the front panel. See Figure 2 on page 22 for an example.

Channel Temperature: All channels should be less than 55 degrees.

NOTE Always have forced airflow across the N1225A whenever power is applied.

Power Supplies: Check that PASSED is shown for all the supplies.

SPI EEPROM Test: PASSED

Internal Com Bus Test: PASSED

Flash RAM Test: PASSED

Loopback Ping: PASSED

Network Ping: Run this test to verify the board can reach another IP address. Enter the IP address and press the Ping button.

Out of Service Tests: Press this button to open a Yes/No dialog box for proceeding to the Out of Service tests.

CAUTION Running these tests can cause permanent loss of position data.

The N1225A Logs Window

Click on the Logs tab and review the N1225A Logs section. Below is a typical set of log entries:

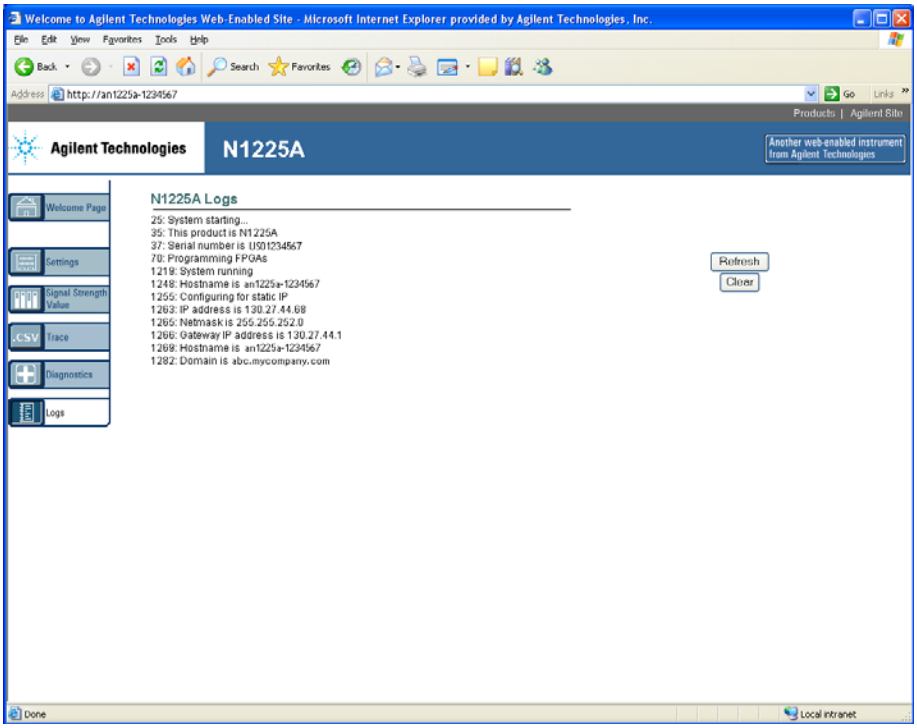


Figure 18 The Logs window

A new log is generated by the on-board microprocessor each time the N1225A is powered up. The log shows the boot-up events. Pressing *Refresh* updates the display. Pressing *Clear* erases the log.

3
Operating the Agilent N1225A

Introduction

This chapter explains how the input and output signals and control registers in the laser axis board work from a block diagram perspective and how to make measurements. It includes basic instructions for reading and writing to N1225A registers and verifying access to the board. It also explains the front panel LED operation and defines the scope probe socket signals. Commonly used terms such as **channel**, **axis**, **sampling**, and **counts** are explained. Which bits to set, sampling modes, where to read the results, hardware position outputs, and what to expect for a basic measurement are also among the topics covered. How to use built-in test generators to simulate results when no laser measurement system is available is discussed. Commonly used setups for making measurements are illustrated as starting points.

Block Diagram & Description of Operation

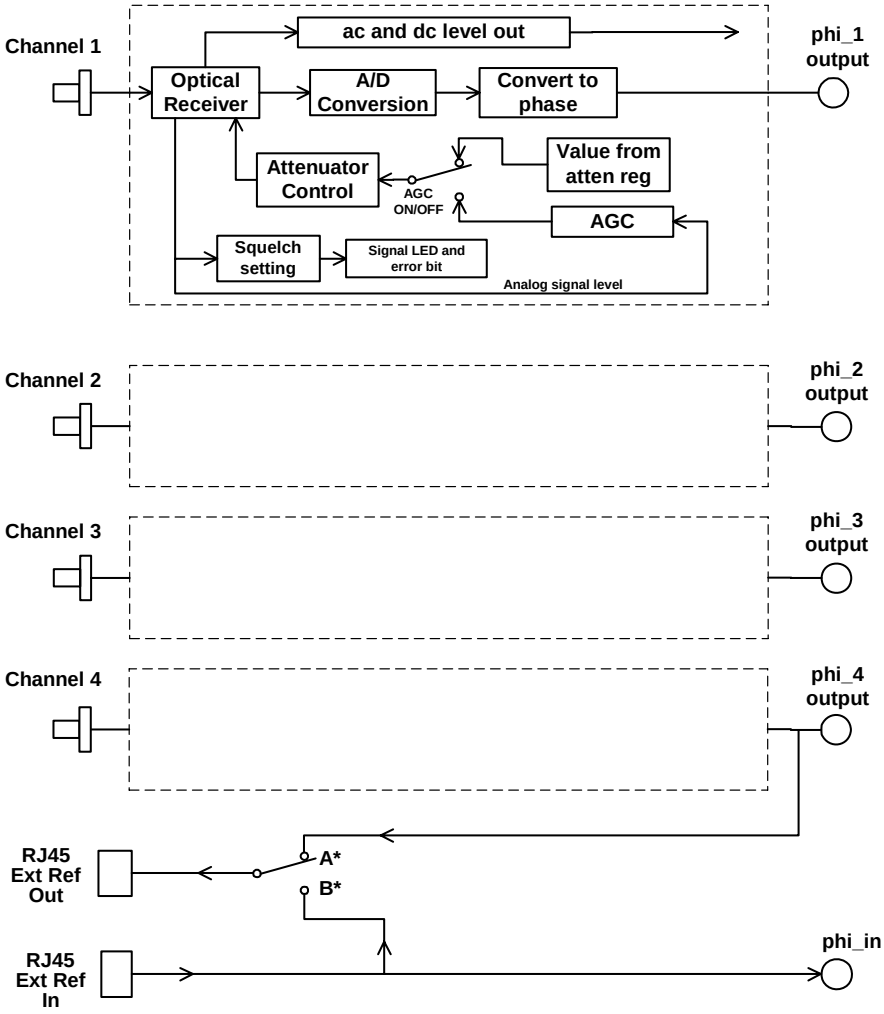
Input circuits

Figure 19 shows the signal path starting at the front panel ST connector. Light is channeled from the optical portions of the measurement system into a fiber optic attached to the ST connector. The optical receiver contains a photo diode to first convert light into a current, then convert it to a voltage in the first stage amplifier. After additional gain stages, the analog voltage is digitized and processed using an Agilent proprietary algorithm to create a phase word for the respective channel. For channel 1, the phase is called **phi_1**. The optical receiver separates the ac and dc components of the input signal. These components are digitized and appear in the channel AC and DC strength registers. The input circuits include an automatic gain control (AGC) which is on by default, and a squelch control. The AGC can be turned off, and the gain controlled using the gain and squelch setting register. On the laser axis board front panel, the first stage optical receiver output is observable by plugging in a 3.2 mm high impedance (10 MHz) probe. This signal can be useful in checking and optimizing the optical alignment.

NOTE

The gain setting affects the observed dc and ac signal level, so turn the AGC off if you want to see relative changes. Channels 1 through 4 are identical in processing their input light signals, but channel 4has a additional purpose. Channel 4 is the only channel wired to create a reference signal output for the REF OUT connector.

The N1225A computes the distance traveled by comparing the phase difference between a reference and a measurement signal. In previous laser axis boards the reference signal came from a receiver built into the laser head itself. In N1225A systems a small portion of the light from the laser head is routed to channel 4 and serves as the reference. For example, in a two-board, one-laser system the phase word from channel 4 can be passed to the next laser axis board using the Agilent supplied reference passing cable. In a three-board system, the middle laser axis board receives the reference from the first board and passes it to the third board.



* When the board is receiving a signal at the Ext Ref In connector the switch is automatically set to position "B", otherwise it is set to position "A".

Figure 19 N1225A input circuit block diagram

Data flow and measurement path

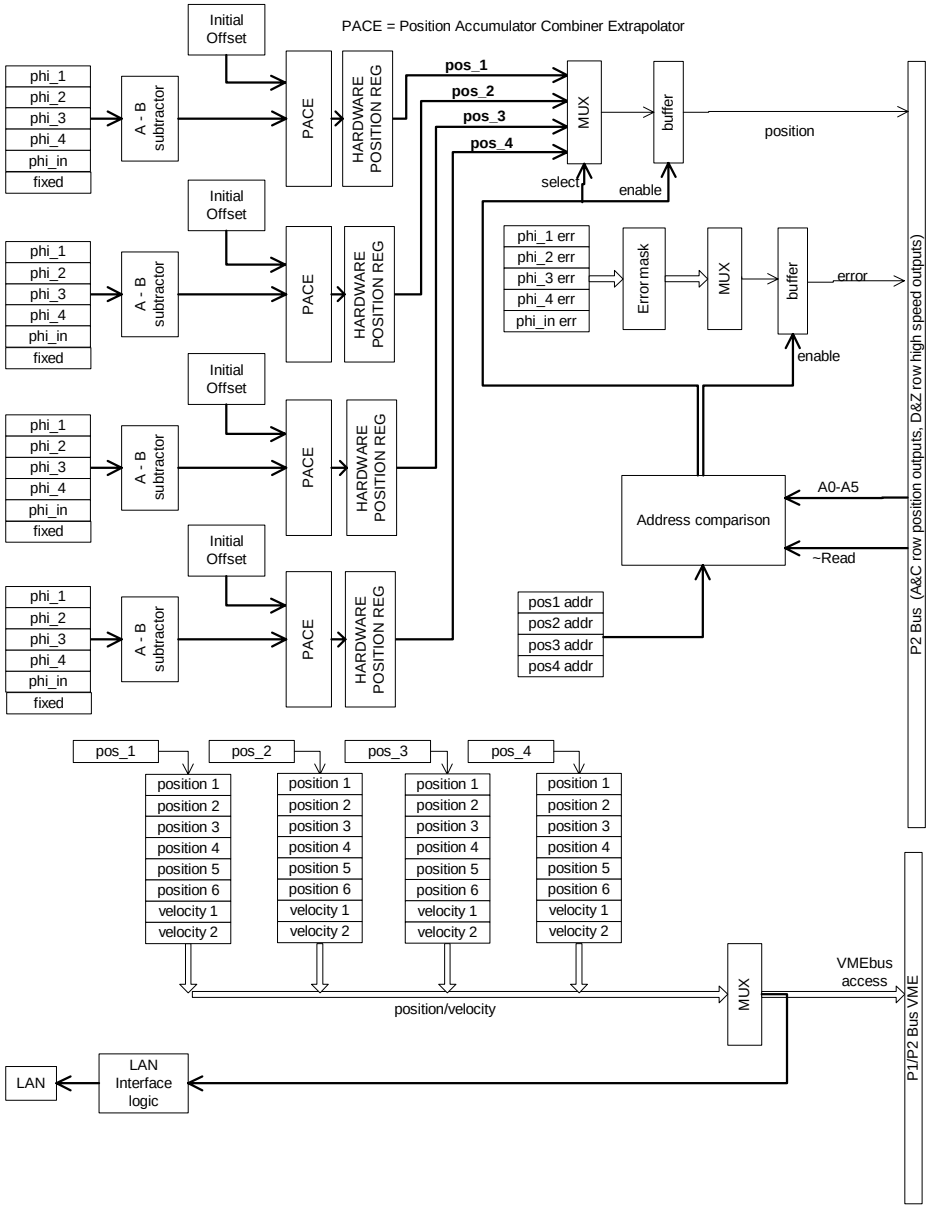


Figure 20 Data flow and measurement path

Figure 20 is a continuation of the previous block diagram, Figure 19. From the left, phase words from the four optical channels, **phi_in**, and **fixed** are routed to the A–B subtractor block. Phi_1 through phi_4 are from optical channels 1 through 4. Phi_in would come from an adjacent board, through the reference passing cable. The fixed phase value, **fixed**, is for testing purposes when no other signals are available.

The input for channel 1 is from the measurement beam of an interferometer in the optical portion of your system. The input for channel 4 comes from diverting a tiny portion of the incident laser light. This is normally obtained near the laser head using a low percentage non-polarizing beam splitter. The phase difference between these two inputs is computed by the subtractor.

The A–B subtractor is programmed using the Laser Source Control registers for each axis. A selection from the six choices is made and then the phase difference between them is output. From the subtractor the phase word goes to the PACE and Hardware Position register. The PACE extrapolates and outputs a new phase word to the Hardware Position register every 100 ns. The phase values accumulate as a 37-bit word, where the LSB is the maximum resolution of the system.

$$\text{System resolution} = \left[\left(\frac{x}{N}\right)\left(\frac{1}{\text{electronic resolution extension}}\right)\right]$$

Where:

x = wavelength of HeNe laser light (≈632.9914 nm)

N = the optical fold factor (OFF)

OFF is an integer value determined by the type of interferometer in the system. For linear optics, OFF=2 and for plane mirror optics, OFF=4.

Electronic resolution extension of the N1225A = 1024

The Hardware Position register can be initialized to zero or an **initial offset** value. From the time of initialization it is updated every 100 ns. Pos_1 is the phase difference between channels 1 and 4 and is referred to as a **measurement axis**. A single laser axis board can have up to three axes, two laser axis boards could have up to seven axes, and so forth. Position is expressed in laser counts, where one count is the resolution of the system. When the N1225A is used with plane mirror optics, one count is 0.15 nm.

For a single board system, pos_1 through pos_3 are the measurement axes with each one computed by subtracting the phase values you choose. If your system uses two boards, the second board usually receives its reference signal through the reference passing cable and will have four axes of measurement.

Each axis has the same options for reading and storing position and velocity values.

The following list of functions can be performed by the N1225A.

- The value of the hardware position register (position) can be stored to one or more position registers, shown at the bottom of Figure 20, for each axis by writing to the command register or by toggling the hardware sample lines either externally or using the command register.
- The axis velocity can be stored in one or more velocity registers in the same way as position.

- A 36-bit position word can be read directly from P2 bus rows A and C. It is updated at 10 MHz, multiplexed between the four axes, so the maximum rate for reading the positions of the axes is 2.5 MHz. In this configuration, a customer provided board places an axis address on rows A and C of the P2 connector and toggles a ~Read line. This causes the laser axis board to send the respective axes position and error status to rows A and C of P2 for latching by the customer board.
- Taking position measurements at regular intervals for readout on P2 rows A and C.
- Position measurements initiated by an external sample line.
- Read 10-bit position words for all axes simultaneously from P2 Z, A, C and D rows. Updated at 10 MHz.
- Two position comparators on each axis can trigger software and hardware notification when the position reaches a value less than or equal to or greater than a value you preset, or if it is between two values.
- Reading a position over the VMEbus.
- Setting up a condition that prevents another position reading from being made until the current position sample has been read over the VMEbus.
- Reading position values for all axes using the LAN port.
- Detection of Error Conditions: Error detection happens early in the measurement process, at the input channels and phase measuring algorithm, then propagates to the error status and reset register. Two error mask registers downstream allow you to decide which errors will affect the P2 bus A row Error pin and D row ~Error Out pin, or which will create a VME interrupt. Error conditions are also readable over VME.
- The N1225A has a DHCP enabled LAN port and embedded web page server. From the LAN port you can read and write to most registers.

Basic Reading and Writing to the Registers

In order to use the information in this section you must know the base address of the laser axis board in the VMEbus backplane. See Chapter 2 for address setting instructions.

Location of data in the VME address space

Each VMEbus address locates 8-bits (one byte) of data. Because the N1225A VMEbus data transfer is specified as D16/D32, data must be read and written 16-bits or 32-bits at a time. This means legitimate 16-bit reads/writes can only be made at even addresses. Figure 21 shows how a 16-bit value is positioned at address location $000000 and $000002 (hex):

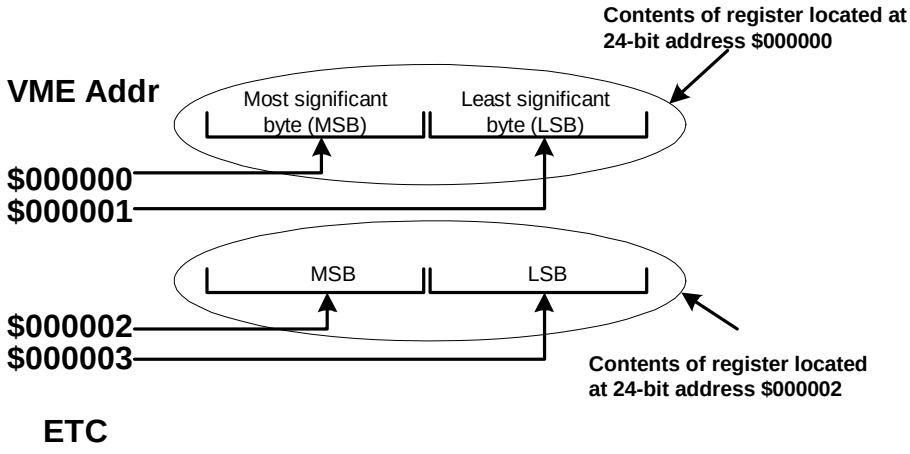


Figure 21 Sixteen-bit values at address location $000000 and $000002

NOTE **Making an incorrect 16-bit read at address $000001, can give a mixed message, the LSB of one register and the MSB of the following register. Always be sure you are reading and writing on the proper word boundaries.**

For 32-bit reads and writes addresses must be divisible by four. In Figure 22, the MSB and LSB are combined into a 32-bit word. In this diagram, the MSW of the top register occupies addresses $000000, $000001 and the LSW is in locations $000002 and $000003. It is the same for the data located at $000004.

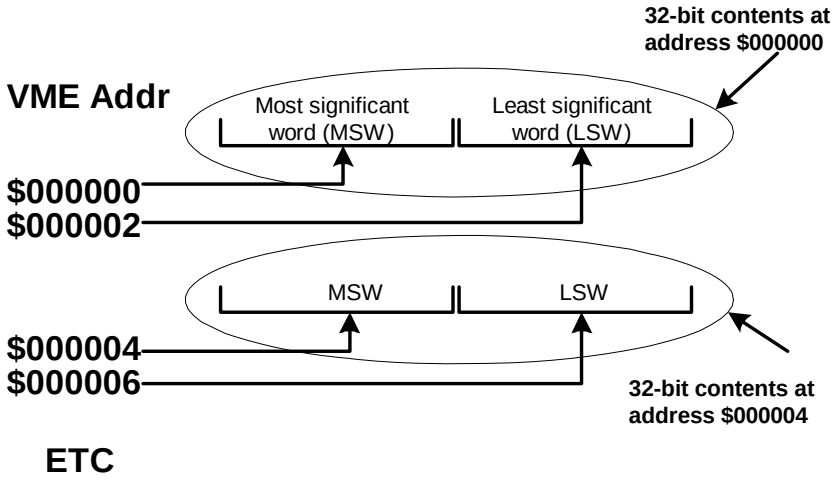


Figure 22 The MSW and LSW are combined into a 32-bit word

Base addresses and register offset

The address switches, S1 and S2 select the type of addressing (A16, A24, A16 and GAP, A24 and GAP) and each board must have its own unique base address. Register addresses in this manual are specified as address offsets. For example, if the board base address is (hex) $001800 and you want to read the least significant word of the Board Level IRQ Error Mask register (a 16-bit value), the absolute address would be computed as shown in Example #1.

Example #1

To compute the absolute address for reading the least significant word, or 16-bits, of the Board Level IRQ register:

Board base address + Address offset for LSW of Board Level IRQ Error Mask register = Absolute address

$001800+ $0000A6 = $0018A6

Example #2

To determining the absolute address for reading the Channe1 1 AC and DC power level register:

Base address of board + Channe1 1 AC and DC power level register = Absolute address

$001800+ $000014 = $001814

Read the 32-bit value at address $001814. The most significant word is the AC power level and the least significant word is the DC power.

NOTE **The address computed in Example 1 only works when reading a 16-bit value, since the address is evenly divisible by 2, but not by 4. In Example 2 the computed read address is divisible evenly by 2 and 4, so this address could be used if you only wanted to read the MSW of the Channe1 1 AC and DC power level register. However, in most cases, performing the 32-bit read is easier than tracking whether the address being used is divisible by 2 or by 4.**

To verify communication with the board over VMEbus

1 An easy way to verify communication with the board is to try reading the first six characters of the MAC address of the board. It is 12 hex characters, starting at address offset $0042. Refer to "Address Maps" on page 165, which shows "reserved" for the 16-bits at offset $0040, then "MAC[5] and MAC[4] at address $0042, MAC[3], and MAC[2] at $0044, and MAC[1] and MAC[0] at $0046. The MAC address is 12 hex characters that are unique to each board. For the N1225A, the MAC address is stated as `00:3C:DC:xx:xx:xx` where "xx: is unique to each board and each "x" is one hexadecimal character. Try reading MAC[5] through MAC[0]. Using 32-bit reads you will see the values shown in the following table. Try again using 16-bit reads.

Address offset	Value	Remarks
$000040	$rr003cdc	rr are the "reserved" bits, ignore the value
$000044	$xxxxxxxx	xxxxxxxx

2 Now write and read back two 32-bit values to the Axis1 Position Comparator High registers located at address offsets $000006C and $000070.

3 Write the 16-bit value $0080 to the General Control and Status register for Axis1, located at address offset $000002. This causes the status LED on the front panel to start flashing. Write $0000 to return the status LED to solid green.

NOTE **These two writes actually clear all the bits in this register. In your program you will want to preserve the value of the other bits when writing to change individual register bits.**

You have now confirmed two-way communications with the board over the VMEbus using 32 and 16-bit reads and writes.

N1225A Front Panel

Front panel LED operation

- Error (Err) LED One per channel (amber).

  This LED lights when these error conditions exist on the channel:

  - ac light power into the respective channel is too high
  - dc light power at the channel is too high
  - ac light power into the channel has fallen below the squelch level (see squelch setting register)
  - a loss of lock condition was detected by phase measurement algorithm for the channel

  Set points for the error conditions are listed in "Board Level Error Status and Reset Register (32-Bit Offset $0028)" on page 112. All of these conditions are latched. This means the LED stays on until the error cause is removed and the error is reset by writing a "1" to the respective bit(s) in the error status and reset register.

- Signal LED One per channel (green).

  Illuminated if there is enough ac light power going into the channel to make a valid measurement.

The signal LED will flash if excessive AC or DC light power is applied to the channel input.

- Status LED One per board (green).

  This LED has two functions. After power up, the Status LED flashes about once/second while the board boots up (less than 30 seconds), then changes to solid green. If there is a bootup error, the LED turns off. After a successful boot, the Status LED is user controllable. You can write a "1" to bit 7 of the axis1 General control and status register to change this LED from steady green to flashing green.

- LINK LED (green) Located in the upper-left corner of the 10/100 Ethernet connector.

  This LED goes on when the Ethernet cable is attached. It lights to indicate that the adapter has received a LNK pulse from the hub, indicating an active Ethernet link. If it is off, there can be cable, connector or hub problems.

- ACT LED (amber) Located in the lower-left corner of the 10/100 Ethernet connector.

This lights when read or write activity is detected on the network, regardless of whether the N1225A is communicating. If the LED is off even after the N1225A has booted, check that your hub and network are operating.

N1225A front panel connections

- Optical inputs Channels 1 through 4

  These connections accept standard ST optical fibers. Use either 400 µ glass or 1 mm plastic fibers. Within these product numbers are options for various length fiber cables: E1705B (plastic Vpin to ST); E1705E (glass Vpin to ST); E1705F(glass ST to ST)

- Scope probe socket Channels 1 through 4

  This fits a 3.18mm (0.125") scope probe, such as the Agilent 10433B Miniature Passive Probe, 10:1, 2 m or equivalent, and is connected to the output of the first stage amplifier. Use a high impedance probe, 10 MΩ or more, to prevent loading the amplifier stage.

NOTE When the AGC is on, it will control the amplitude of this signal.

If you are using the signal amplitude during alignment, turn the AGC off and manually set the channel gain.

- Ref OUT One per board

  Applies to a multi-board system where many axes share a common reference. The optical reference fiber is connected to the ST connector of channel 4 of the first, or master, board in the reference passing chain. An Agilent supplied reference passing cable connects Ref OUT of this board to Ref IN of the next board. The master board automatically detects it is the master and no register settings are needed. Boards downstream from the master determine their position in the chain, which is enumerated in bits B0 thru B3 in the board reference ID register. The master board is board zero.

- Ref IN One per board

  When multiple boards are used with one reference, the reference is daisy chained from board to board using an Agilent supplied reference passing cable. Ref IN receives a digitally coded reference and clock from the adjacent board.

- 10/100 Ethernet

Standard 10/100 Base T(x) LAN port. By default, this port is DHCP enabled when shipped, but DHCP can be turned off, and a static IP address and 15-character host name can be assigned. The MAC address can be found on a board label on the circuit side of the board next to P1 and P2 and read from the MAC address register.

Front panel reset button

Hold the reset button down for greater than five seconds to restore the board to the factory default conditions. See Figure 3 on page 23 for the location of the reset button. Use a paper clip to access the reset button through the 1 mm hole near the words 10/100 Ethernet.

NOTE

If you are prompted to enter a user name and password, which can occur after using the RESET button to restore the board to factory default conditions, the defaults are:

User name: N1225A

Password: N1225A

N1225A Optical Channels

Channel AGC, gain, squelch and power

By default, the automatic gain control, AGC is on, and controls the gain of the channel amplifiers, adjusting it to match the light power coming into the ST connector. While AGC is on, the gain value being applied can be read from the Channel X gain setting register by reading the three LSBs. There are four possible gain settings, which are enumerated by the three LSBs in this register. To turn AGC off, specify a gain value by writing to the three LSBs of the Channel X gain setting register and to restore AGC, write zero to these same bits. State of the AGC is retained in non-volatile RAM when the board is off.

The squelch works by comparing the AC light power going into a channel with the squelch value loaded into the Channel X squelch setting register. When AC power is below the squelch setting, the front panel signal LED for that channel will be amber, and the Power below squelch error bit for the respective channel in the Board level error status and reset register will be set and latched.

The light power going into each channel is measured and expressed as AC and DC values in the respective channels' AC and DC power level registers. One 32-bit read brings in both power levels as two concatenated 16-bit words. Apply a conversion factor specified in the Register Bit Descriptions section of this manual to get power in μW. Power levels read from these registers are approximate and the accuracy varies over a wide range depending on the power coming into the channel. The power level read in the power level registers is adjusted for AGC. Power levels are updated at 100 Hz.

To simulate the presence of optical signals

To simulate a stationary position for test purposes, writing hex 55 to the source control register for a channel forces phase to be fixed at zero for that channel. Combining this with writing to the preset position register allows setting the position counter for that axis to any arbitrary value. Once the position counter is set, it can be sampled in a variety of ways and the values output over the P2 user defined rows and read over VME or through the LAN port. However, setting channel 4, the reference channel, to zero does not cause a phase value of zero to be sent over the reference passing cable. Writing hex 55 also causes a value of 5 μW to be read from the AC and DC power level registers for that channel.

Sampling/Reading Data over VME

To sample

Each axis has one hardware position register which holds the current position in laser counts for its axis. **Sampling** or **to sample** means copying the contents of this register to another location for reading over the VMEbus or P2 hardware outputs

The hardware position register has 37 bits. Based on the required resolution, measurement range, and maybe wanting to use only a 32-bit read per sample, you can select a contiguous 32-bits out of the 37 available in the hardware position register by setting appropriate bits in the respective axes Output Control and Status and Setup registers. However, all 37 bits are still available.

Each axis has six position and two velocity sample registers as shown in Figure 23. These registers are read over the VMEbus. For faster data output with more uniform control of data age, there are hardware outputs over the P2 bus which are updated at a maximum 10 MHz rate.

NOTE

Sampling, copying the Hardware Position register contents to the Position/Velocity Sample registers, can be initiated from a hardware input by bringing one or more ~Sample lines LOW, or software by initiating a sample with a write to the axis command register using VMEbus or over the LAN via the web browser.

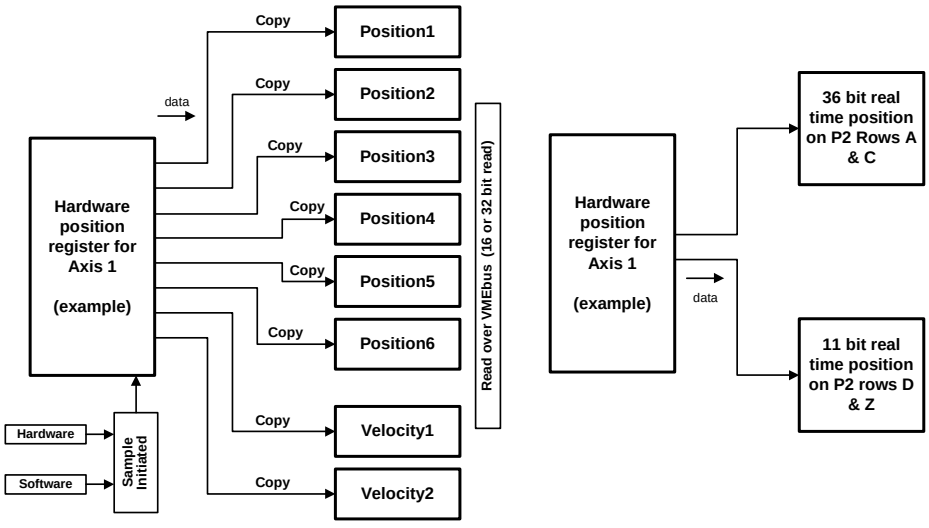


Figure 23 Position and Velocity Registers

To auto-sample

Auto-sampling reads and captures data with a single VMEbus command. Auto-sampling is performed by reading an **alternate address** with an offset that is $0040 greater than the Position or Velocity register. With auto-sample, reading the high-order byte in the **alternate** Position or Velocity register updates the position or velocity value in the respective register. For example, the axis 1 Position1 alternate register for auto sampling is located at: $0044 + the offset of the axis 1, Position1 register equals $0144. Reading the MSB of this alternate register causes position to immediately be sampled and written into the alternate Position1 register. You get a sample every read without the overhead of writing to take a sample followed by reading to read the value.

NOTE

Completion of the read cycle is delayed by up to 150 ns so the sample operation can finish, allowing the auto-sample operation to return the value just sampled. This is different than the 10897/8 operation where the value sampled is not available until the next read operation.

To sample with VMEbus or hardware

To sample a single axis using a VMEbus command: Write a “1” to the bit corresponding to the position and/or velocity registers you want to use in the respective axis command register. This forces the Hardware position register value to immediately be copied to the specified sample registers. Read the register values over the VMEbus any time after the sample command. The copied value remains in the Position or Velocity registers until it is updated using the described procedure.

To sample using an external hardware trigger and read through software: Drive the desired TTL ~Sample1 through ~Sample4 pins on the P2 connector LOW. This causes the hardware position register contents for each axis to be written to the Position1 through Position4 registers respectively. Read these registers any time after the sample.

To capture multiple axes simultaneously with a VMEbus command: Write a “1” to a Drive Sample bit in the Command register. This causes the board being addressed to drive its defined ~Sample pins on the P2 connector to output a ~Sample signal that can drive the ~Sample inputs of other N1225A boards. Read the captured Position or Velocity register values of the boards one by one over VMEbus. For a standard VME backplane an A and C row overlay is needed to bus these signals between all the boards.

To control the reading and taking of data sampled using VMEbus or hardware

Any of the following techniques can be applied to control reading and taking data as described in “To sample with VMEbus or hardware" on page 68.

- Use interrupts to notify the processor that a sample is ready. To generate an interrupt when the sample is ready, set the corresponding IRQ enable bit in the Sample Mode and Mask register, and turn interrupts on after setting the IRQ vector. The user provides the interrupt service routine to check the sample status register or other registers and take the appropriate action.
- Use repeated reads of the Sample Status register. When a sample is ready, the corresponding bit in this register is set. Reading the data clears the bit. For slow sample rates a loop can monitor this register and call a read subroutine when new data is available.
- Simultaneously sample Position and velocity. Position1 and Velocity1, and Position2 and Velocity2 registers can be simultaneously sampled in pairs by using the Hardware Sample Mode bits in the General Control and Status register.
- Avoid lost data points. Setting the corresponding Sample Mode Bit in the Sample Mode and Mask register will prevent a position or velocity register from being updated until after the sample has been read, even if a sample request has been sent multiple times. Figure 24 is a flowchart for the sample mode and mask bits.

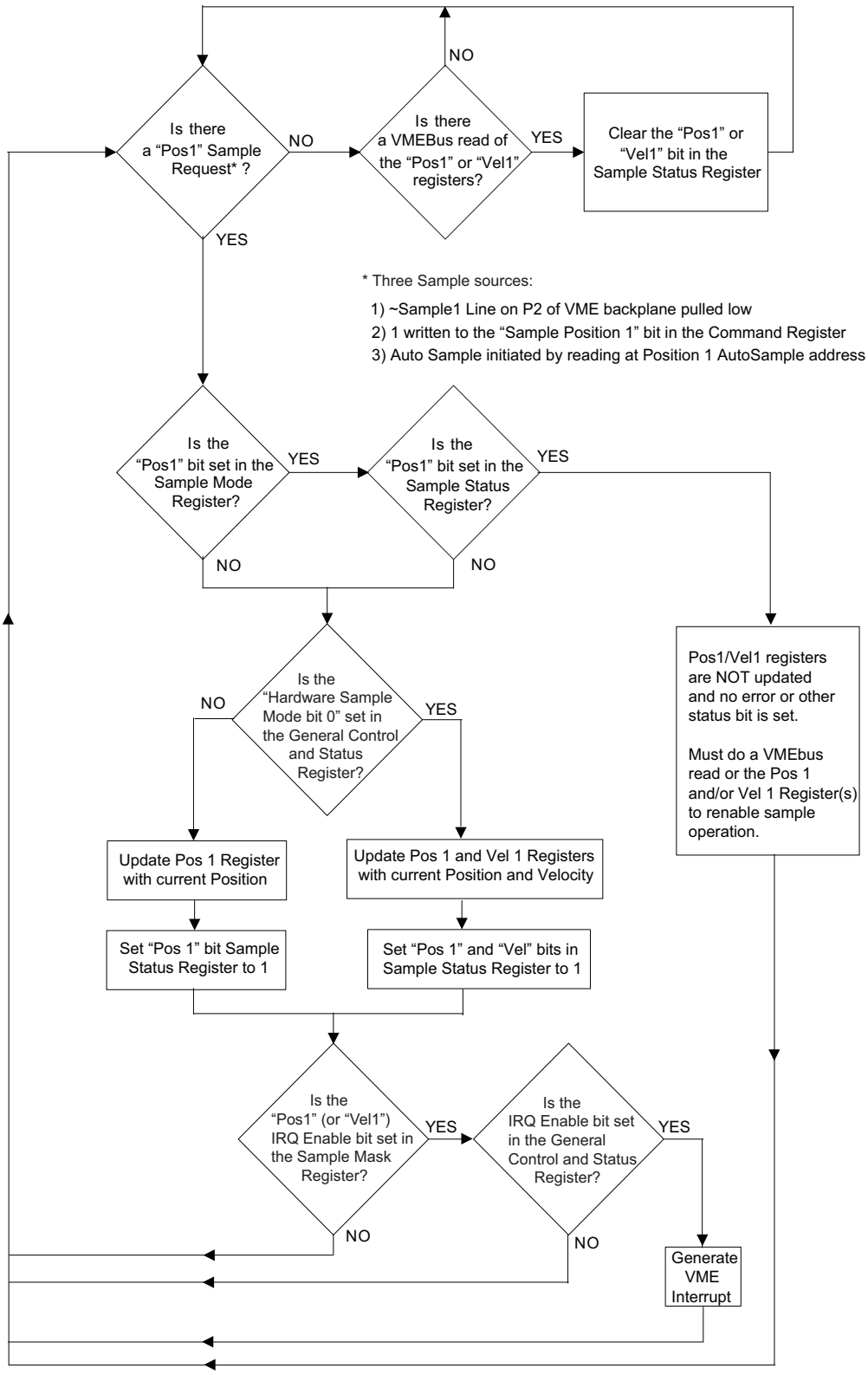


Figure 24 Flowchart of the Sample Mode and Mask Bits

Sampling/Reading Data Off the P2 Bus Rows D, A, C, and Z.

Background

While digital position can be read using the VMEbus alone, it is asynchronous and relatively low speed. For this reason, an alternative synchronous digital data path exists through the outer rows (Rows D, A, C, and Z) of the P2 backplane connector. This Hardware Position bus is for high-speed and multi-axis applications. It can be configured to provide real-time position data output synchronized among multiple N1225A boards. This section refers to hardware position words and other TTL signals on the P2 user defined pins. Data read off these rows of P2 is accessed completely independent of the VMEbus. Typically the N1225A is communicating over the backplane with customer specific proprietary hardware. Refer to Chapter 5, "Hardware Interface," for P2 bus pin-out information and termination requirements.

Thirty-six pins on the P2 A and C rows provide an addressable hardware position word for each axis. To use this function for axis1, for example, load a 6-bit address into the Axis1 Output Control and Status register 0 for bits A5–A0. Ensure that each axis for all of the boards on the backplane has its own unique A5–A0 address to avoid bus contention and possible damage. Next, set the "All axes P2 bus data output enable bit" in the Axis 1 setup register. From now on, when P2 bus address pins A5–A0 match what is loaded in the register, and the ~Read line is brought LOW, the laser axis board will put position onto the bus (P2 rows A and C), and drive the Error line. Position will update every 100ns, the maximum rate for one axis. See Chapter 8, "Specifications for timing.

Ten-bit high speed parallel outputs on the P2 D, A, C, Z rows provide all four axes of position simultaneously updated every 100 ns. This is for applications demanding a very high data rate with relatively low axis velocity requirements. All four outputs are turned on by setting bit B4 in the Axis1 Setup register. See Chapter 8, "Specifications for timing.

To simultaneously sample using Asynchronous modes in multiple board systems

- The purpose of the Async Modes is to provide simultaneous Hardware Position sampling and synchronous data transfer by one or more laser axis boards. This reduces data age uncertainty and differences between axes that might occur if these axes were clocked out on different clock edges. Two P2 signal lines working together provide this function: AOH/OCLK and Output Hold. There are three basic ways to use these lines:
- Control by an external asynchronous signal (Async Mode 0).

- Control by an external asynchronous signal which is automatically synchronized to the 10 MHz clock (Async Mode 1).
- Control by the local 10MHz clock, either divided down by some factor or used at 10 MHz (Async Modes 2 and 3).

Since one board will do the controlling and the others will be controlled, both the AOH/OCLK line and the Output Hold must both be configured as either outputs or inputs depending on whether a particular board is a controller or controlled. There is only one controller board but there can be many boards that are controlled. Keeping the purpose of Async Mode clearly in mind and examining Figure 25 shows how this is accomplished.

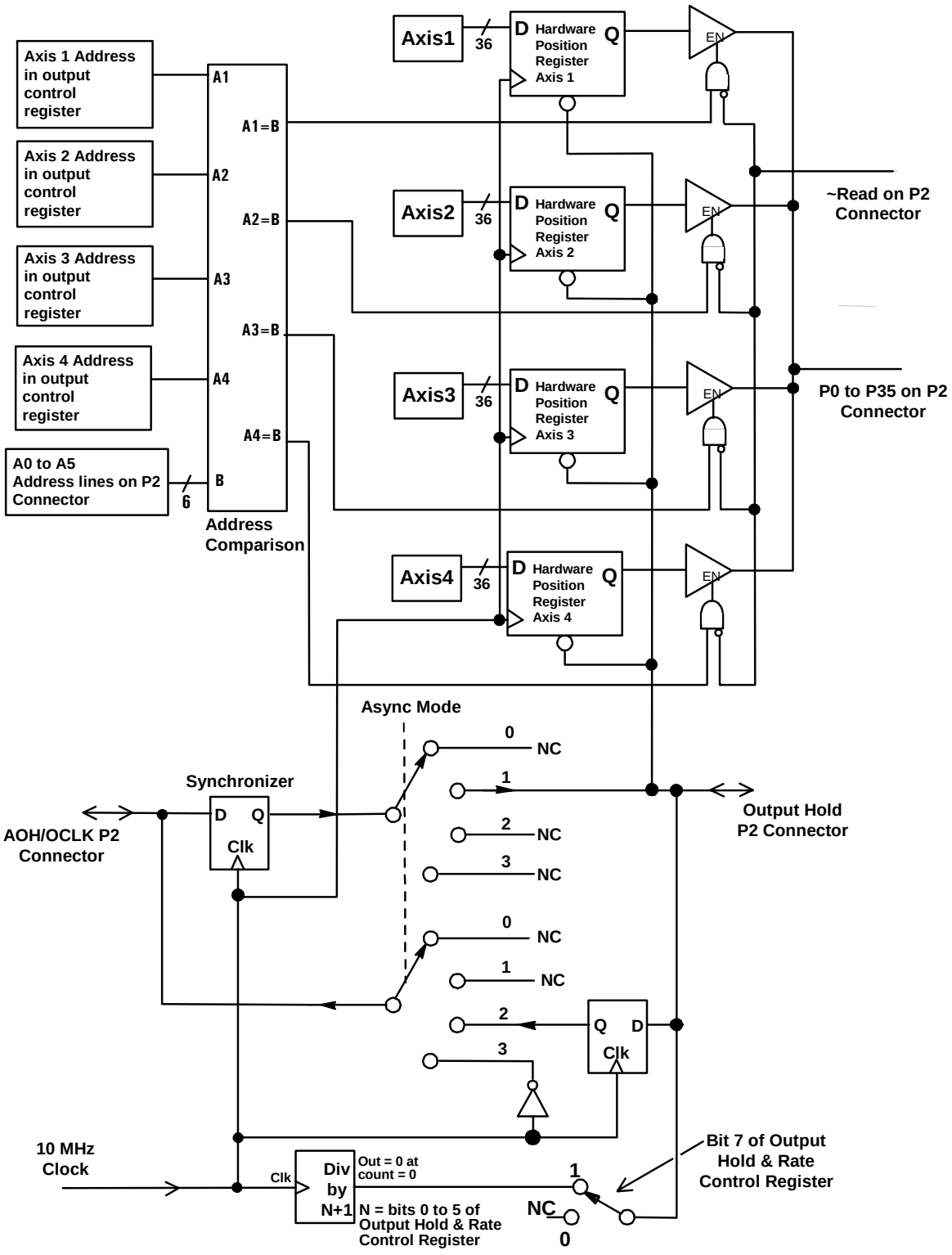


Figure 25 Async mode and P2 logic

This a complete diagram of the Async Mode logic and its connection to all four axes on the N1225A. From this diagram it can be seen that two virtual switches are involved in the setup, one labeled Async Mode and one labeled Bit 7 of Output Hold & Rate Control. In typical multi-board applications, one board is configured for asynchronous mode 1, 2 or 3 and provides synchronizing signals over the P2 A and C rows, and multi-axis cable. The remaining boards are in asynchronous mode 0.

Asynchronous mode 0

If the Async Mode switch is set to position 0 and the Bit 7 of the Output Hold & Rate Control register is set to zero, Async Mode is inactive. This isn't entirely accurate because the Output Hold line still connects all axes of the laser axis board and typically is connected to other boards. More accurately, this is “passive Async Mode” and it is the preferred mode for a controlled board.

Asynchronous mode 1

The first active mode is Async Mode 1 where the Async Mode switch is in position 1. In this mode, the AOH/OCLK line will be treated as an asynchronous hold input that gets synchronized so on the next occurring 10 MHz clock edge Hardware Position data is locked and continues to be locked for as long as AOH/OCLK remains HIGH. Furthermore, the Output Hold line is driven (becomes an output) so the Output Hold lines (treated as inputs) of other controlled laser axis board may be tied to this one so that these also lock their Hardware Position data on the same clock edge. The system may then sequentially read these out while they are being held, confident that all of the data outputs were captured at the same instant and have the same data age. It might appear that simply driving the Output Hold line from an external source would accomplish the same thing but this is not the case. If the asynchronous Output Hold signal happens to split a 10 MHz Clock edge, some boards *might* latch the data at the clock edge but some *might not* latch until the next clock edge. It is better to use the AOH/OCLK line. As shown in Figure 25, this mode requires that Bit 7 of the Output Hold & Rate Control register be set to one to avoid a contention on the Output Hold line. In addition, as mentioned above, a good compatible mode for the N1225A controlled boards is Async Mode 0.

Asynchronous mode 2

In this mode, the laser axis board becomes a controller board clocking Hardware Position data out at a 10 MHz divided by N+1, rate. It drives both the Output Hold line and the AOH/OCLK line, which now becomes a data output clock to your system. The AOH/OCLK output is delayed by one clock period so that it only clocks out valid data. Bits 0 to 5 of the Output Hold & Rate Control register determine the update rate which is 10 MHz divided by N+1, where N is the number in bits 0 to 5 and must have a value in the range of 1 to 63. This mode may only be used for a reduced clock rate provided by a divisor of 2 to

64. If you want to clock data out at a 10 MHz rate, use Async Mode 3 described in the following subsection, "Asynchronous mode 3." Bit 7 of the Output Hold & Rate Control register is set to one so that the internal clock divider drives the Output Hold line that is connected to the controlled boards and X and Y channels. The controlled boards are set to Async Mode 0.

Asynchronous mode 3

In this mode, the laser axis board becomes a controller board clocking Hardware Position data out at the 10 MHz Clock rate. It drives both the Output Hold line and the AOH/OCLK line, which now becomes a data output clock to the user's system. The AOH/OCLK output is delayed by one-half clock period so that it only clocks out valid data. Bits 0 to 5 of the Output Hold & Rate Control register are set to zero and bit 7 is also set to one so that the Output Hold line is also driven by 10 MHz Clock. As before, the controlled boards are set to Async Mode 0.

Figure 25 shows that Async Mode is a board function rather than a single axis function. Therefore, it can be set only for the board. The mode can be set by writing to the Axis 1 Output Control register.

To use the Output Hold Line to reduce the data rate

The laser axis board generates Hardware Position data at a 10 MHz rate, but this rate may be reduced by using the Output Hold line. For example, the Output Hold line can be programmed to assert for N × 100 ns, then de-assert for one cycle (100 ns), where N is a number from 0 to 63. Or, the Output Hold line can be driven externally, providing user control of sample rate. Bit 7 of the Output Hold & Rate Control (OHRC) register controls this. If Bit 7 is cleared, the output rate generator *does not* drive the Output Hold line and you may be able to drive the Output Hold pin of P2 externally, depending on which Async mode the board is in. If Bit 7 is set, the Output Hold line is driven by the laser axis board and you must not attempt to drive it. It should be evident from Figure 25 that the OHRC register sets a board level function affecting all axes, and cannot control individual axes. Values are set by writing to the Board Level OHRC register. A VMEbus SYSRESET of the laser axis board will initialize the OHRC register to zero. Following are more details about Async modes and the Output Hold Line.

To drive the Output Hold line externally, load the OHRC register with decimal zero and set the board for Async mode 0. Bringing the Output Hold line HIGH prevents the Hardware Position register for all axes from being updated (it holds the current position).

To use the AOH/OCLK pin as an asynchronous hold input, load the OHRC register with decimal zero and set the board to Async Mode 1. When the AOH/OCLK line is brought HIGH, it will be synchronized to the board clock, driving the Output Hold line HIGH and causing the Hardware Position register for all axes to hold the current position.

To cause the laser axis board to drive the Output Hold line at a rate of [10/(N+1) MHz], load the OHRC register with the value N, where N = 63 or less, set bit 7 and set the board to Async mode 2. The Output Hold line will be driven HIGH and held for (N × 100ns), then go LOW for 100 ns. While Output Hold is HIGH, the Hardware Position register for all axes holds the current position.

To cause the laser axis board to drive the Output Hold line at the 10 MHz Clock rate, the OHRC register is set to decimal 128 and the board is set to Async mode 3. This causes the Hardware Position register to be updated every 100 ns for all axes.

To use the high speed parallel position outputs

Position output for all four axes is available simultaneously at a 10 MHz rate, but with a reduced number of bits (10 LSBs). These position outputs are on P2 rows D, A, C and Z. Because of the reduced number of bits, there is a velocity limit of less than 768 mm/s plane mirror. The 10 MHz clock can be used to clock this data into external equipment. All four axes are turned on by setting bit-5 in the Axis1 setup register.

NOTE

The following pins, connected to the 74LVTH125 parts, when used as inputs must be driven or have pull-up resistors to ensure a minimum current to the pin of 0.5 mA: Force Zero Input, ~Sample1-4, ~Position Reset, Output Hold, ~Read Input, AOH/CLK I/O. If this is not done the input logic state is unknown.

Synchronizing Multiple Boards to the Clock

The laser axis board has an internal clock or can be clocked from an external 10 MHz source via the P connector as shown in Figure 26. This is usually done to synchronize data being read off the P2 connector with external boards latching the data. The laser axis board can also supply a 10 MHz clock. However, unlike previous VME laser axis boards, multiple N1225A laser axis boards are synchronized using the reference passing cable. For example, to synchronize two or more laser axis boards to the backplane 10 MHz clock, you would install the reference passing cables and set the first board to take its 10 MHz reference from the backplane. The other N1225A boards will be synchronized over the reference passing cable and should not be programmed to take their 10 MHz off the backplane. In fact, boards that are slaves are prevented from receiving 10 MHz over the backplane. Time delay in the reference passing cable is automatically compensated.

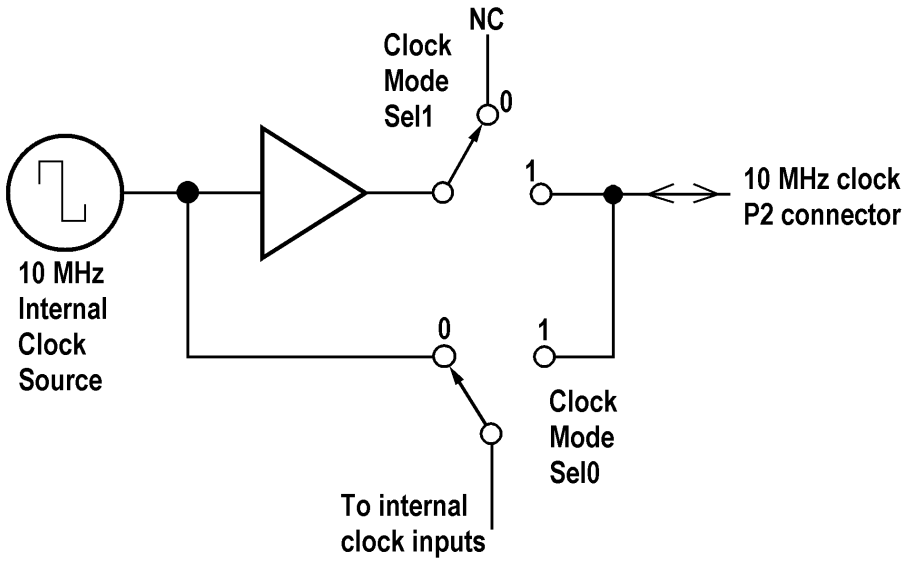


Figure 26 Clock mode operation

Clock source

In Clock Mode 0, the default, the laser axis board uses its internal clock and does not drive the 10 MHz Clock In/Out pin on the P2 connector. Clock mode 1 uses a 10 MHz external clock and in Clock mode 3 the board uses its internal clock and drives the P2 bus with the same clock. Clock mode is a board level function, and set using bits Clock Mode Sel1 and Clock Mode Sel0 in the Board Level Output Control and Status register.

Initializing the Position Counter

Each axis has its own position counter, command register and General Control & Status register. The position counter holds a random value on power-up. Writing 1 to the Reset Position bit in the command register sets the position counter to zero or to the value in the axes position preset register, depending on the state of the Preset Enable bit in the General Control & Status register for the axis.

The Position Counters continually updates the position value for each axis. On startup, the position counters hold a random value that is later set to zero or a predetermined value during system initialization. A hardware line or software command can zero, or preset, the Position Counter.

To set the Position Counter to zero using software:

1 Clear the Preset enable bit in the axes General Control and Status register.

2 Write 1 to the Reset Position bit in the axes Command register.

To reset the Position Counter using the P2 A row ~Position Reset line using hardware

1 Clear the Preset enable bit in the axes General Control and Status register for all axes you want to reset.

2 Pull the ~Position Reset line (pin P2-A7) LOW. All axes which have their Preset Enable bit cleared in their General Control and Status register will have their position counters reset to zero.

NOTE Zeroing an axes position counter via hardware is not qualified by the A0 to A5 address pins of P2 or any other signal.

To reset the Position Counter of an axis to zero using the P2 Z row reset line

1 Set the D Row Reset Enable bit in the respective axis Setup register.

2 Drive the Axis Reset In line on the P2 Z row HIGH. The PC for the respective axis will be reset.

To set the PC to a predetermined value using software

1 Set the Preset enable bit in the axes General Control and Status register (GCSR).

2 Write the required preset value into the respective axis' Position Preset register. Note that the LSB of this register is 0.15nm.

3 Write “1” to the “Reset Position” bit in the axes CR. The Position Preset register value will be written to the PC for the axis.

NOTE

The Position Preset register was the Position Offset register on the 10897/8 boards. On the N1225A it is only used to hold the Position Preset value as this board does not implement a position offset function for the P2 hardware position outputs.

To set the PC to a predetermined value using hardware

1 Set the “Preset enable” bit in the axes General Control and Status register (GCSR).

2 Write the required preset value into the respective axis' Position Preset register. Note that the LSB of this register is 0.15nm.

Pull the ~Position Reset line, P2-A7, low. All axes that have their Preset Enabled bit set in their GCSR will have their PCs set to the value in the Preset register.

NOTE

If the backplane does not have a pull-up resistor for pin P2-A7, it will be interpreted as zero. This can make it impossible to reset, or preset, position when the backplane position preset is enabled and P2-A7 is allowed to float.

Error Detection and Handling

The 32-bit Board Level Error Status and Reset register provides monitoring of critical measurement conditions. Errors that indicate bad data are checked every sample and will latch the data not valid bits. If an error is detected, it is cleared by writing “1” to the bit indicating the error. Certain bits in the Board Level Error and Status register (BLE&SR) are the ORed combination of other error bits.

To troubleshoot the root cause of an error, check the lower level bits before writing “1” to reset the error condition. Setting the Data Not Valid bit after the cause of the error has been removed will also reset the bit(s) that lead up to the Data Not Valid bit being set.

Each bit in the Board Level Error Status and Reset register is described below.

Channel [4 3 2 1] AC too high: There are no lower level bits for this condition. This bit is set and latched when AC power into the channel is above 70 μW. This condition will cause the Data Not Valid bit to be set for any axis that uses the channel where the error occurred.

Channel [4 3 2 1] DC too high: There are no lower level bits for this condition. This bit is set and latched when DC power into the channel is above 187.5 μW. This condition will cause the Data Not Valid bit to be set for any axis that uses the channel where the error occurred.

Channel [4 3 2 1] below squelch: There are no lower level bits for this condition. This bit is set and latched if the AC power into the channel is below the value in the squelch setting register for the individual channel. Power below squelch will NOT cause the Data Not Valid bit to be set.

Channel [4 3 2 1] Loss of Lock: This bit is set and latched if the algorithm cannot follow the input signal phase, or a high APD temperature is detected, which shuts down the channel. Either condition will cause the Data Not Valid bit to be set for any axis that uses the channel where the error occurred.

Backplane 10 MHz Loss of Lock bit: There are no lower level bits for this condition. This bit is set and latched if the backplane 10 MHz clock input is being used and the PLL cannot track the clock signal. This will cause the Data Not Valid bit to be set for all axes on all boards that are daisy chained together, because a possible result is incorrect latching of P2 backplane data.

Reference Error bit: This bit is set and latched when there are problems with the digital reference passed from the adjacent board over the Reference Passing cable. It is the ORed combination of bits in the Reference Error register. This bit does not monitor any conditions on the board that receives the optical reference (Master board).

Axis [1 2 3 4] Position or Velocity Comparator bit: This bit is set and latched when the respective axis position or velocity reaches or exceeds the criterion defined in the Comparator Configuration register. These bits do not affect the validity of any data.

Axis [1 2 3 4] Position Overflow bit: This bit is set and latched when the respective axis position counter over or underflows. It does not affect the Data Not Valid bit.

Axis [1 2 3 4] Data Not Valid bit: This bit is set and latched to indicate that data being supplied by an axis is invalid and is the ORed combination of these bits:

{Channel X AC Too High bit}
{Channel X DC Too High bit}
{Backplane 10 MHz Clock bit, if used}
{Reference Error bit (for slave boards}
{High APD Temperature bit} (which results in the channel being shut down)

NOTE

For a multi-board system, an error on the reference channel of the master board will propagate to all boards in the reference chain. To reset the system after this error, start by resetting errors on the master board, then reset errors on boards in the reference chain, starting with the first board in the chain and proceeding to the last.

- There is one board level IRQ error mask register that specifies which of the detected errors will generate an interrupt.
- Each axis has its own P2 Error Mask register that specifies which of the detected errors will cause the error line on the P2 connector to become active.

The Comparator Function

Each axis has position and velocity comparators that can be set to provide notification when axis position is above, below or between two values. The comparator outputs are available through software and hardware.

The Comparator Configuration register for each axis has bits to define various ways of comparing position or velocity values to values loaded into the Position or Velocity Comparator registers (see Chapter 4, “Comparator Configuration Registers”).

NOTE The values in the Position and Velocity Comparator register are always in LSBs (0.15 nm plane mirror for position and 94.3 nm/s for velocity).

To prevent inadvertent triggering when writing to the comparators, always write the least significant word, the lowest 16-bits, last. For example, with 16-bit writes, write the extended bits first, then the MSBs, and then the LSBs. The entire register is updated when the LSBs are written.

The Trace Function

The trace function works via the web interface and is like having a storage oscilloscope to record position vs. time for one to four axes. Recording begins when the trigger conditions are met, and up to four triggers are used to initiate data collection. Each trigger has a choice of Trigger Off, VME Error, P2D input pin, falling edge, P2D input pin, rising edge and Comparator. Up to 720,896 data points can be recorded prior to the trigger.

Table 5 Summary of Trace Capabilities

Maximum number of data points	720,896 total points captured
Maximum number of data points you can record prior/after the trigger event	Up to 720,896 before the event Up to 700,000 after the event
Sample rate	(312.5 kHz/N) N= 5 to 512 (integer values)
Number of triggers (trace begins when all trigger conditions are simultaneously satisfied)	Up to four separate triggers
Choices available for each of the four triggers (T1 through T4)	Trigger Off VME error P2D input pin, falling edge P2D input pin, rising edge Comparator
Output data file type	*.csv, using DOS (CR-LF) or Unix (CR) line terminators
Data file format	See sample below Figure 37 on <Cross Reference Color>page 93.
Manual triggering?	Yes
Initiate Trace over VME	No
Read Trace data over VME	No

To Use the Trace function

1 Begin by accessing the N1225A through the web interface, then select Trace from the left hand tab. A window similar to the one shown in Figure 27 opens.

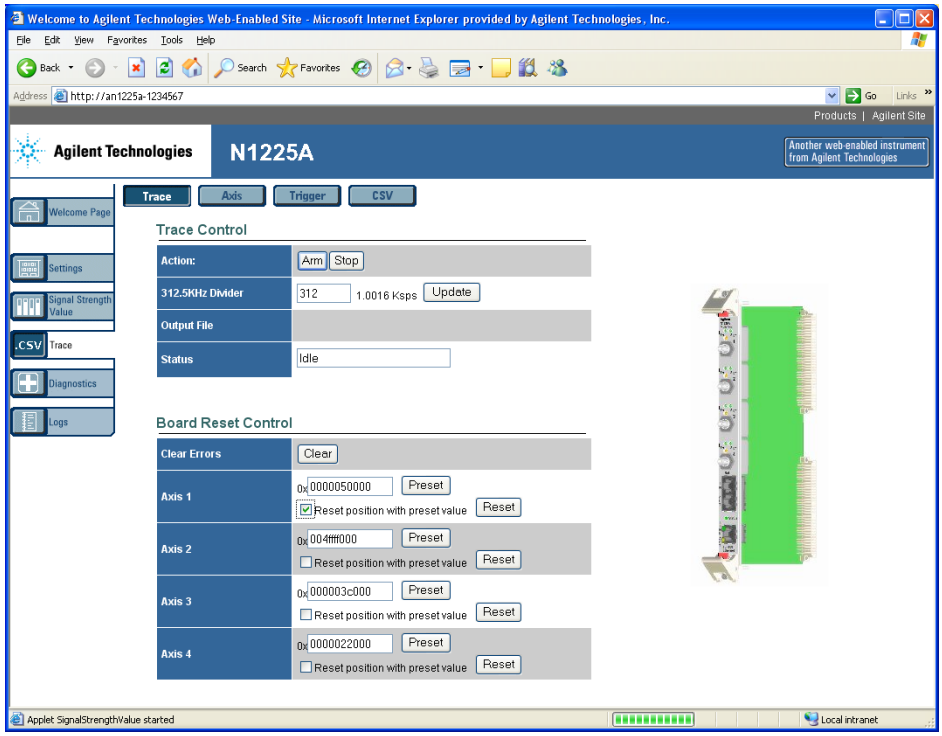


Figure 27 Trace Control web page

2 Check to see if the Update button is grayed out. If it is *not* grayed out proceed to step 3.

If the *Update* button *is* grayed out, a measurement is already in progress. For example, the trigger condition was not met for a previous measurement and the board is waiting for a trigger. Before trying to set new conditions, click *Stop* to abort the measurement.

3 Check the Status field, then click on *Stop* if it shows anything other than "Idle". It needs to indicate idle before any changes can be made to the configuration.

4 Next, set the sample rate by entering an integer value from 5 to 512 in the 312.5 kHz Divider field and then click Update. The sample rate is updated to the new value.

5 The Test Name field is initially blank, and is filled using the CSV screen. After the data is recorded it resides on the N1225A board until downloaded. Clicking on the File Name to open a a dialog box to rename the file and transfer it to your hard drive.

6 The Board Reset Control section, shown in Figure 28, has buttons to clear board errors, clear axis position and preset axis position.

WARNING Any values entered here will change the value read over VMEbus or via the P2 connector and could potentially cause equipment damage or an error if the N1225A is controlling a stage when the Reset button is pressed.

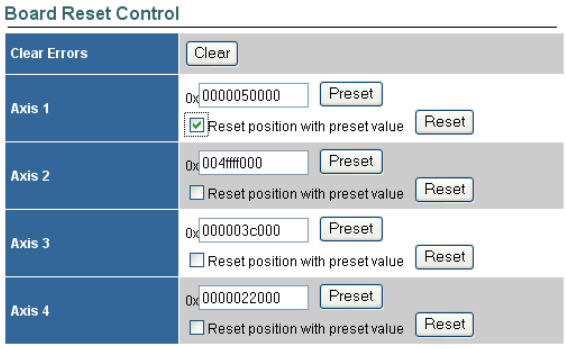


Figure 28 Board Reset Control

The *Clear* button is for clearing latched board errors without resetting axis position.

An axes position can be set to zero by pressing the Reset button. This also clears latched errors on the axis, provided no error conditions are still present.

To preset an axis position and clear errors on that axis, first enter the position value in the field opposite the Preset button, then click the Preset button to update the field. Next, select the Reset Position With Preset Value box, and click the Reset button. The axis position is set to the value in the Preset field and latched errors on that axis are cleared.

To choose the axis to record

1 To select the axis to record, click the Axis button. A window similar to Figure 29 opens.

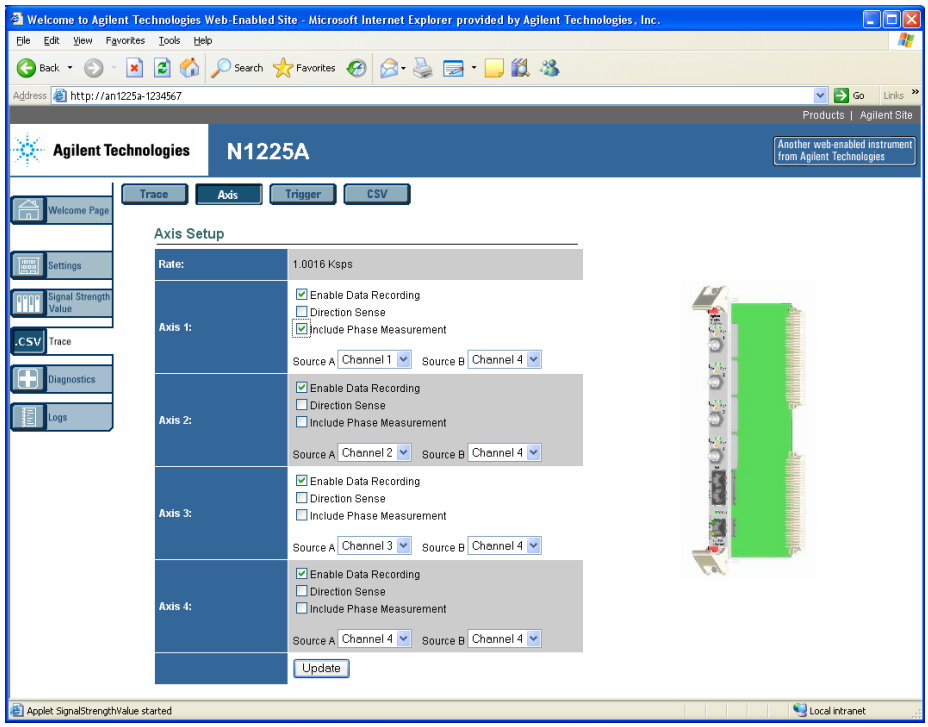


Figure 29 Axis Selection Page for Trace

WARNING Source A and Source B values in Figure 29 are what is in the Laser Source Control register (LSCR) bits B0 through B7. Changing Source A, or Source B or changing direction could cause equipment damage or an error if your stage is being controlled using N1225A data (over P2 or VMEbus) when the LSCR is changed. The LSCR for all axes is updated to the new values when you click the ***Update*** button.

2 Click to select Enable, Direction or Phase for the axes being recorded. Checking Enable causes axis position to be recorded, and enables it for triggering. Putting a check mark in the Enable and Direction boxes reverses the direction sense for the axis and for data read over the VMEbus or over the P2 connector. Refer to the warning above. Checking Phase causes accumulated phase, raw laser counts, to be stored. At least one axis must be selected for data recording to occur.

3 Source A and Source B select the channels that will be subtracted to obtain axis position. Any changes here will change the Laser Source Control

register and most likely cause a jump in measured position. Choices are: Channel 1, Channel 2, Channel 3, Channel 4, External Reference and zero.

4 Click *Update* to store your changes.

To setup the trigger

1 Click the *Trigger* button to open a window similar to the one shown in Figure 30. This window allows the individual trigger conditions to be set. It also is used to choose how many trigger conditions have to be met before starting to take trace data.

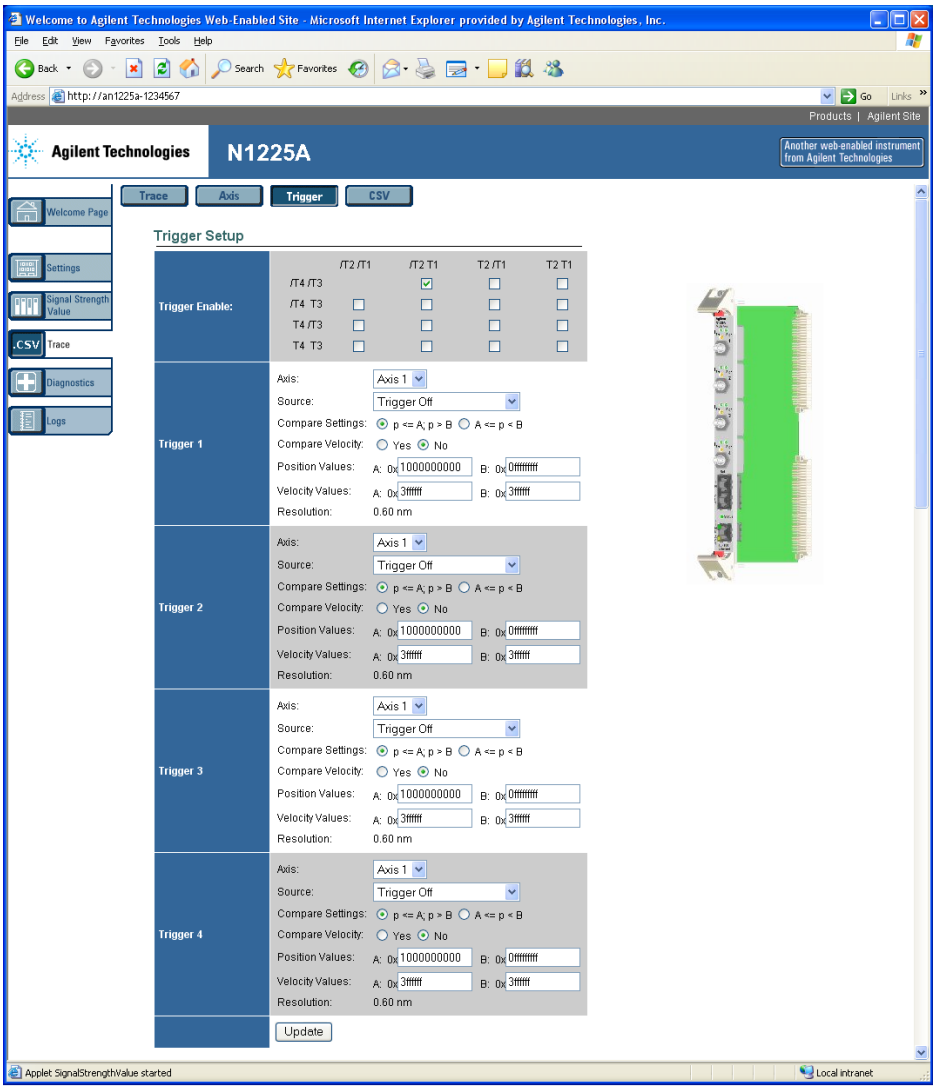


Figure 30 Trace Trigger Page

Setting the Trigger Enable conditions

1 Locate the Trigger Enable section in Figure 30. It contains 16 check boxes representing all possible combinations for four trigger conditions.

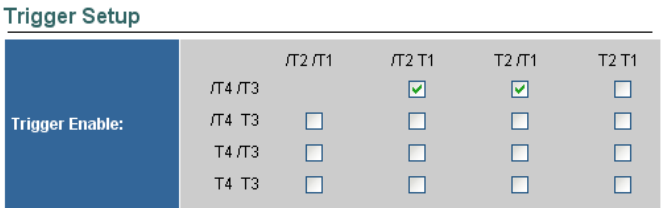


Figure 31 Trigger Enable Section, Trigger on T1 T2 T3 T4

Figure 31 is a close-up view of the Trigger Enable section.

2 Click a box, or boxes, to set up a logical condition for triggering.

For example, select the box in the lower right corner, at the intersection of T2, T1, T3, and T4, to require all four trigger conditions must be met simultaneously before data will start to be recorded.

When multiple boxes are selected, their logical conditions are ORed together. For example, in Figure 31, triggering is enabled if either T1 or T2 is a logical “1”.

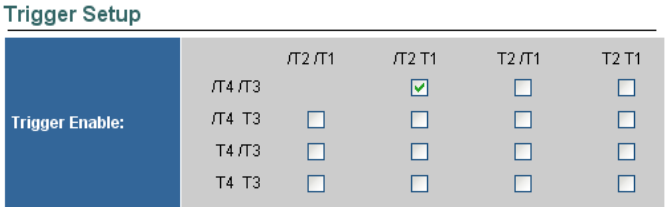


Figure 32 Trigger on T1

Figure 32 shows triggering configured for T1 only. It assumes that Trigger Off is selected as the source for Triggers 2, 3 and 4. Setting Trigger Off for these trigger conditions sets them to logical ”0”. The ‘/’ negates the logical zero, making it logic ‘1’. In the table, the ‘X’ is in a location where T2, T3, and T4 are True because of the logical negation. T1 remains logical ‘0’ until its trigger condition is met. Then, when the T1 trigger condition is met:

- T1 becomes True, logical ‘1’
- The trigger condition for trace to begin, (/T4 AND /T3 AND /T2 AND T1), is met
- Data recording starts.

Setting up a trigger using the comparator

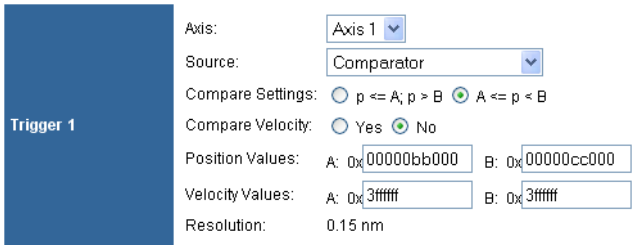


Figure 33 Trigger 1 using Comparator

In the Trigger 1 section shown in Figure 33, “Trigger 1” is logical “1” when the position of Axis 1 is between $0000bb000 and $0000cc000. When position is outside this window, the logical value is “0”. Axis Velocity is not considered in this case.

Setting Source to “Trigger Off” would set the Trigger value to logical zero.

If velocity were selected, then both position and velocity are examined and are ANDed together, so both conditions have to be met to generate a trigger. The velocity condition is satisfied when $A < v \leq B$.

Selecting a trigger source

Figure 34 shows the choices available for trigger sources. You can choose Axis 1 through 4 as the position value being examined to create a trigger, and for the Axis, choose events on that axis that could generate a trigger.

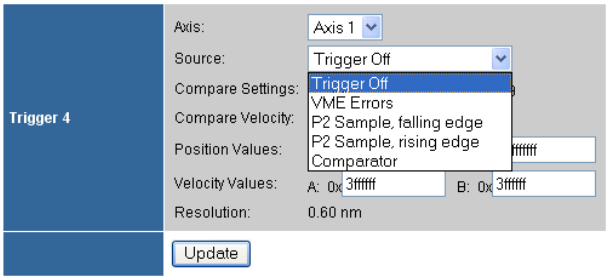


Figure 34 Trigger Selection

1 Select one of the following as the source.

Trigger Selection panel

Trigger Off

Trigger Off sets the trigger value to logical “0”.

VME Errors

Trigger value is “1” whenever an error condition in the VME Error Status registers associated with channels used for the selected axis occur. For example, if Axis 1 is chosen for triggering, and Axis 1 = Channel 1 minus external reference, then only VME errors occurring on channel 1 or external reference are considered. Remember that each channel has its own VME Error Status registers.

P2D input pin falling/rising edge

The trigger value goes to “1” when a falling (or rising) edge is detected on pin P2-D12 (P2D_IN1). This trigger source is shared among all axes and is not associated with any one axis.

Comparator

When axis position and/or velocity is within (or outside) a comparator window, the trigger value is “1”, otherwise it is zero. Triggering can also occur when axis velocity exceeds a setpoint.

2 After setting the trigger conditions, click Update to save the settings.

To use the CSV screen.

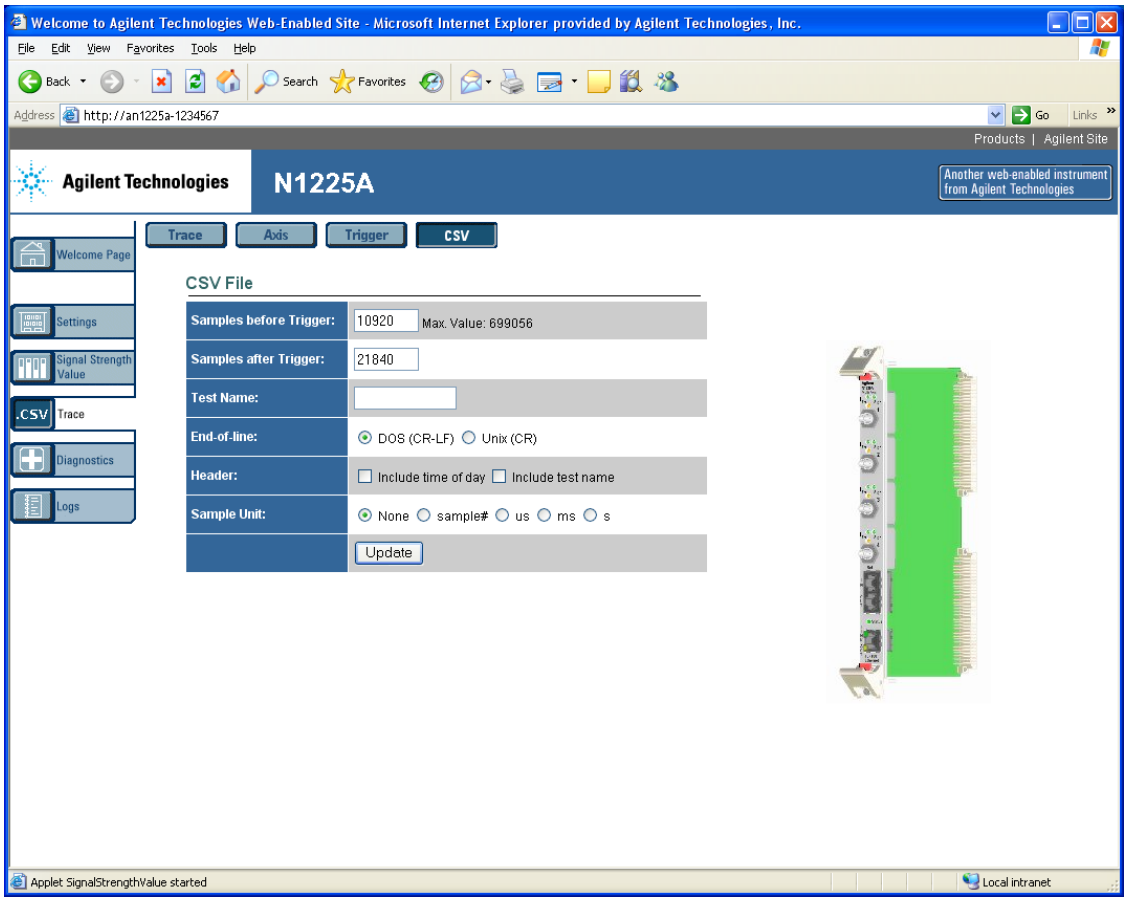


Figure 35 CSV Screen for Trace

1 The Setting Samples Before Trigger field allows you to position the data relative to the trigger point. Enter the number of samples to be recorded before the trigger.

2 The Setting Samples After Trigger field allows you to position the data relative to the trigger point. Enter the number of samples to be recorded after the trigger.

   For example, setting Samples before trigger to 250,000 causes 250,000 data records to be recorded before the trigger point and continuing until the “Samples after trigger” requirement is met.

   Trace memory holds over 700,000 data points. If one axis is being observed, all the values can be allocated to that one axis. If tracing 2 axes, over 350,000 points per axis are available and so on.

3 In the Test Name field enter a custom filename, if desired. The custom name will appear in the Trace screen. The N1225A assigns a random name ending

in .csv to each data file. You may use the random filename or assign a new name when downloading data to your hard drive.

4 Select either DOS or Unix in the Use the For End of Line field to select either a carriage-return-line-feed for DOS or a carriage-return for UNIX after each line or record, including records for Time-of-Day and "Test Name". The data values within the record are separated by commas for both DOS and Unix files.

5 The Header field lets you select either Include Time of Day" to use the computer clock or an NTP server to provide date and time. The date and time correspond to when the stop button on the Trace page was pressed as the last step in recording the data.

To include the test name at the beginning of the .csv file, select "Include Test Name".

6 Before exiting this screen click Update to save the settings.

Returning to the Trace Control web page

1 Click Trace to go back to the Trace Control web page, and click Arm. This readies the board to record data when the trigger condition is met.

The Status box will change from "Idle" to "Armed". When the trigger conditions are satisfied, the Status box changes momentarily to "Un-armed" then to "Retrieving Post-store", then "Done (click stop)", indicating the data is ready to be downloaded.

2 When the Status box reads Done, click the Stop button and wait for the filename to turn blue, and be underlined. The status box will change to "Idle", indicating the data is available from the N1225A embedded server application.

3 To download the data from the Trace Control page by click on the Output File Name.

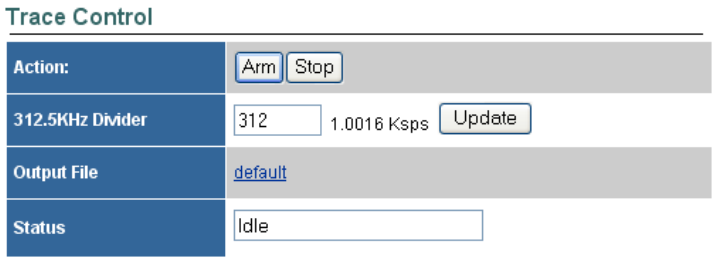


Figure 36 Trace Control Box

4 Click on the Output File Name to open a File Download dialog box. The file can now be loaded to your hard drive. It can also be renamed.

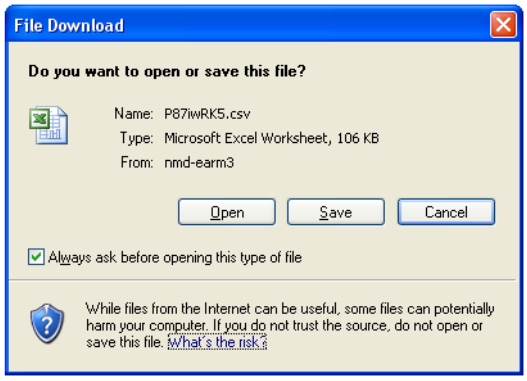


Figure 37 File Download dialog box

A sample of the data record for Axis1 phase data is shown below:

```
Test rate [Hz],39062.5000   this line shows sampling frequency
Sample#,,phi1,Pos1    sample number, phase, for Axis 1
0,15728640            actual data - sample number, phase value
1,15728640
2,15728640
3,15728640
4,15728640
5,15728640
```

This completes the process of taking a trace.

To initiate a trace manually

To initiate a trace manually, set up the comparator so axis position is within the window. Then when the trace is armed it will immediately start collecting data. For a manually initiated trace, the first data point is taken when the trace is armed, no data points are recorded prior to the time the Arm button is pressed on the Trace screen.

Processing Delays

In applications where position signals are constantly changing because the system providing the position signals is moving, and depending on the accuracy requirement, it is sometimes necessary to take into account the short processing delay introduced by the laser axis board. This delay is the time required to convert an incoming position signal to an output digital value. It consists of the accumulated time for:

- The measurement signals to propagate from the input connectors through the measurement electronics
- The phase difference to be calculated
- The Position Counter value to either be copied to a Position register or transferred to the Hardware Position output on the P2 bus.

VMEbus Sample Delay and Data Age

The value of the processing delay through the processing chain described above and into the Position registers is nearly constant and is accurately known. The processing delay for the laser axis board is 2951 ns from arrival at the board inputs to insertion into a Position register.

The VMEbus processing delay represents the minimum possible time interval between the occurrence of a new measurement signal at the board input and the instant at which the generated position value can be read over VMEbus from a Position register. At some time between the time of arrival of the measurement signal and the time of transfer to a Position register, the user initiated sampling signal occurs that causes the new position value to be latched into the register. The sampling signal is typically provided by a HIGH to LOW transition of a signal on one of the P2 ~Sample pins. This signal is an inverted enable on an internal latch that transfers the data synchronously on the next positive edge of the 10 MHz clock. We identify this clock transition as the sample time. With reference to the sample time, it is useful to consider the VMEbus processing delay as being composed of two separate intervals, one prior to the sample time and one after.

The first interval, known as the data age, is the interval between time of position signal arrival and the sample time. It has acquired this name because it can be thought of as the age of the data that will be transferred to the Position register at the sampling instant. Then the position data is transferred to a Position register some integer number of clock periods after the signal is sampled. Consequently, this second time interval is known as the **sample delay**.

Although the total VMEbus processing delay is constant and is always 2951 ns, it is possible to adjust the split between the sample time and sample delay. For example, adding more delay in the sampling signal path moves the sampling signal closer to the time of arrival of a new position signal and simultaneously lengthens the sample delay.

To provide for special requirements such as, for example, autosampling, the laser axis board provides two possible sample delay settings for each Position and Velocity register. The delay value is programmed by setting a bit in the Sample Delay register. Each bit of this register determines the sample delay for a different Position or Velocity register. The Sample Delay register bit for a particular Position or Velocity register has the effect shown in Table 6.

Table 6 Sample Delay Register Bit

Sample Delay Bit	Data Age (ns)	Sample Delay (ns)
1	2951	100
0	251	2800

You should interpret the sample delay to be the earliest time at which the sample value is available for transfer over VMEbus relative to the sampling time (that is, the positive 10 MHz clock edge following the HIGH to LOW transition of a P2 ~Sample pin signal).

The Auto-Sample feature is a special case that requires a short sample delay. This is necessary because the start of a VMEbus read triggers immediate sampling at the next positive-going 10 MHz clock edge. The resulting output value must be available quickly so the present read cycle can finish. This is guaranteed by setting the Sample Delay bit to one in order to program a sample delay of 100 ns. See “Sample Delay Register" on page 156 for additional details and the Sample Delay register bit assignments.

P2 Data Age

As with the VMEbus sample delay, the value of the processing delay through the processing chain and onto the P2 Hardware Position output is also essentially constant and is accurately known. The processing delay for the N1225A board is very close to 3051 ns from the time of arrival at the board inputs to synchronous transfer of the numerical value at the P2 outer row pins. Specifications on the variation of this value can be found in “Digital Interface" on page 236.

Sample delay is not applicable to the Hardware Position register outputs accessible over the P2 outer rows because P2 ~Sample signals are not used to transfer position data to P2. Instead, position data is continuously updated at positive clock transitions of the 10 MHz clock. Consequently, the P2 data age is equal to the P2 processing delay. As above, the data age can be thought of as the age of the data at the instant of transfer onto the P2 bus by a clock edge.

10/100 BaseT(x) LAN

The N1225A has a LAN connection so it can be accessed remotely over your network. For security purposes, have a firewall between the network and the laser axis board.

Web server

The N1225A contains a web page server providing a bar graph display of signal levels, squelch setting and other functions. (Sun JavaVM needs to be installed in order to use the N1225A web interface.) Through the web interface you can update board firmware and view log events and errors. Read/write access to some board registers is also available through the LAN using a rudimentary interface. For alignment, a bar graph showing relative signal levels is displayed in the web page. The VMEbus controller is not needed in order to use the LAN interface, only a +5 Volt supply to the board.

CAUTION Always have the specified airflow whenever power is applied to the board. A safety shutdown to protect the APD is incorporated in the board design, but do not rely on it to prevent damage. Temperatures above 60° C in the APD area, see Figure 2 on page 22 identifying the APD area, with power applied will permanently damage the APD and lower the sensitivity of the board. The board will have to be returned to the factory for expensive repairs. See the maintenance and service chapter for more information.

MAC and IP address

The LAN connection supports both DHCP and static IP addressing. The board is shipped configured for DHCP and is restored to DHCP when the Reset button is pressed.

Each laser axis board is labeled with a MAC address (see Figure 3 on page 23); also readable over the VMEbus. If DHCP is used or the static IP address of the laser axis board is unknown, send a “ping” using the hostname, a combination of the model and serial number in the format “an1225a-XXXXXXX” where XXXXXXX is the last seven digits of the product serial number, will reveal the IP address providing the network has a DNS server. The hostname can be changed on the Setup web page or in VME registers.

NOTE

In some cases, you will have to append domain information to the hostname.
For example, `ping an1225a-`*`6061234.eed.mycompany.com`*, where:
6061234 = the last seven digits of the N1225A serial number
eed.mycompany.com = your domain

To change from DHCP to static IP addressing using the VME bus

1. Write the desired IP address, SNM and GIP to the respective registers.
2. If desired, set the hostname value.
3. Set bit-4 in the LAN configuration register, with bit-0 set to 0. This sets a static IP address.
4. Verify bit-4, Static IP accept, in the LAN status register is set.

To change from static IP addressing to DHCP using the VME bus

1. With the board connected to the LAN, write “1” to the DHCP enable bit in the LAN configuration register.
2. Wait about five seconds to allow activity over the LAN to complete.
3. Read the LAN status register and verify that bit 0 (DHCP Enabled) is set.

NOTE

The length of time required to allow activity over the LAN, nominally five seconds, depends on LAN traffic and DHCP server latencies. Read the IP address register or ping using the board hostname to determine the assigned address. Success or failure of “pinging” using the hostname depends on the DNS server.

To change from DHCP to Static IP addressing from the web interface

1. Select the Settings tab on the N1225A Welcome page.
2. Click the DHCP: Off button
3. Fill in the following fields:

   Hostname: [strongly recommended]
   Domain name: [May leave blank]
   IP Address: [required]
   Netmask: [required]
   Default Gateway: [recommended]
4. When you are done entering data in the fields, click the Update button.

NOTE

If the IP address, or hostname, has been changed, the connection between the web page and the board will be broken. Reestablish communication by entering the IP address or hostname into the address field of your browser.

To change from Static to DHCP addressing from the web interface

1 Select the Settings tab on the N1225A Welcome page.

2 Click the DHCP: On button

3 Fill in the following fields

Hostname: [optional, but highly recommended]

4 When you are done entering data in the fields, click the Update button.

(The board will be assigned a new IP address by the DHCP server. Use the hostname in your browser to reestablish communications with the board. If no hostname was assigned, you will need to log into your router to see what IP address was assigned, or as a last resort, try a reverse arp lookup.

Using the N1225A in Place of Other Boards

In many cases one N1225A can replace two 10898A or four 10897x boards, and their accompanying receivers and cables. The P2 row A and C hardware interface is also designed to be compatible with systems using the 10897/98 boards. The pin-out, addressing, operation of Error and Read lines is the same as these previous boards. For software, each axis uses $0200 of address space, like axes on the 10897/8 boards and for most registers, bits and bit locations are the same, and they work similarly.

Figures 38 and 39 show systems using the 10898A and N1225A.

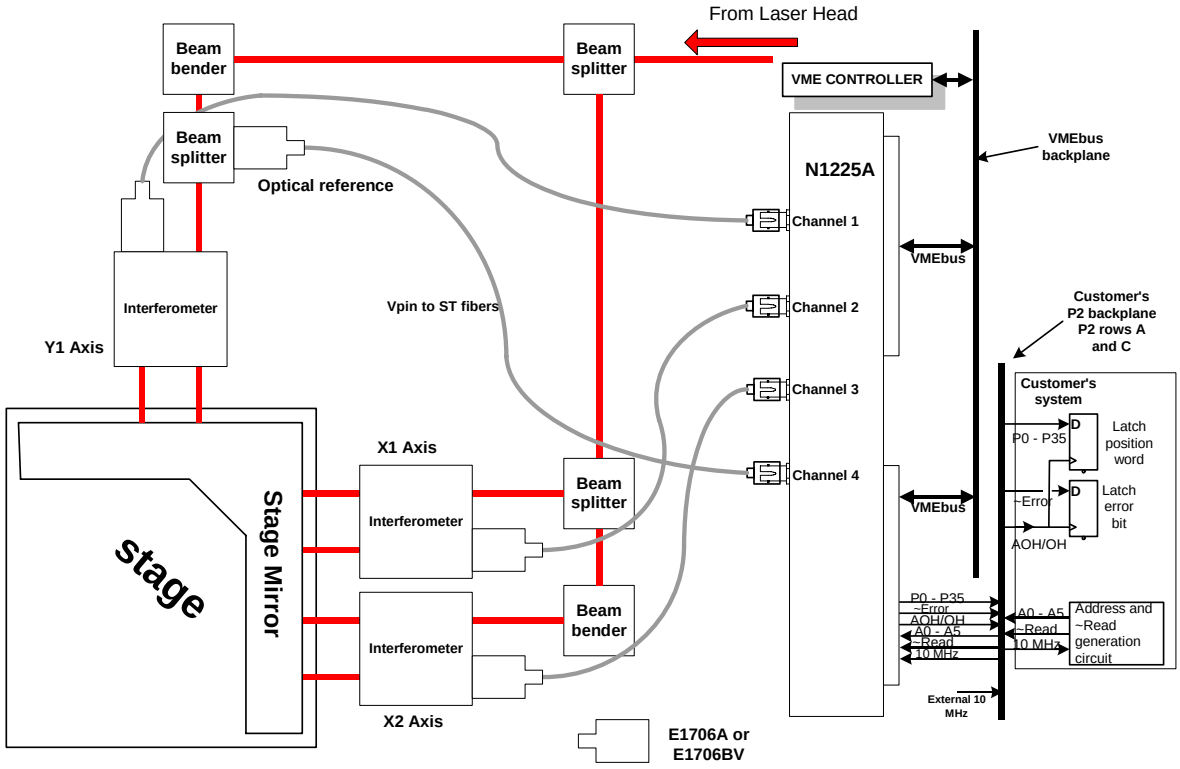


Figure 38 Optical setup for both the N1225A and 10898A

The optical layout is a basic three axis XY stage, with a rotation measurement being made in the X direction and an additional beam splitter to sample a portion of the incident laser beam. A fiber routes this signal, called the optical reference, to channel 4 of the N1225A. Systems using the 10897/8 laser axis boards use an electrical signal from the laser head that's derived from sampling a portion of the exit beam and using a comparator to create a square wave electrical reference.

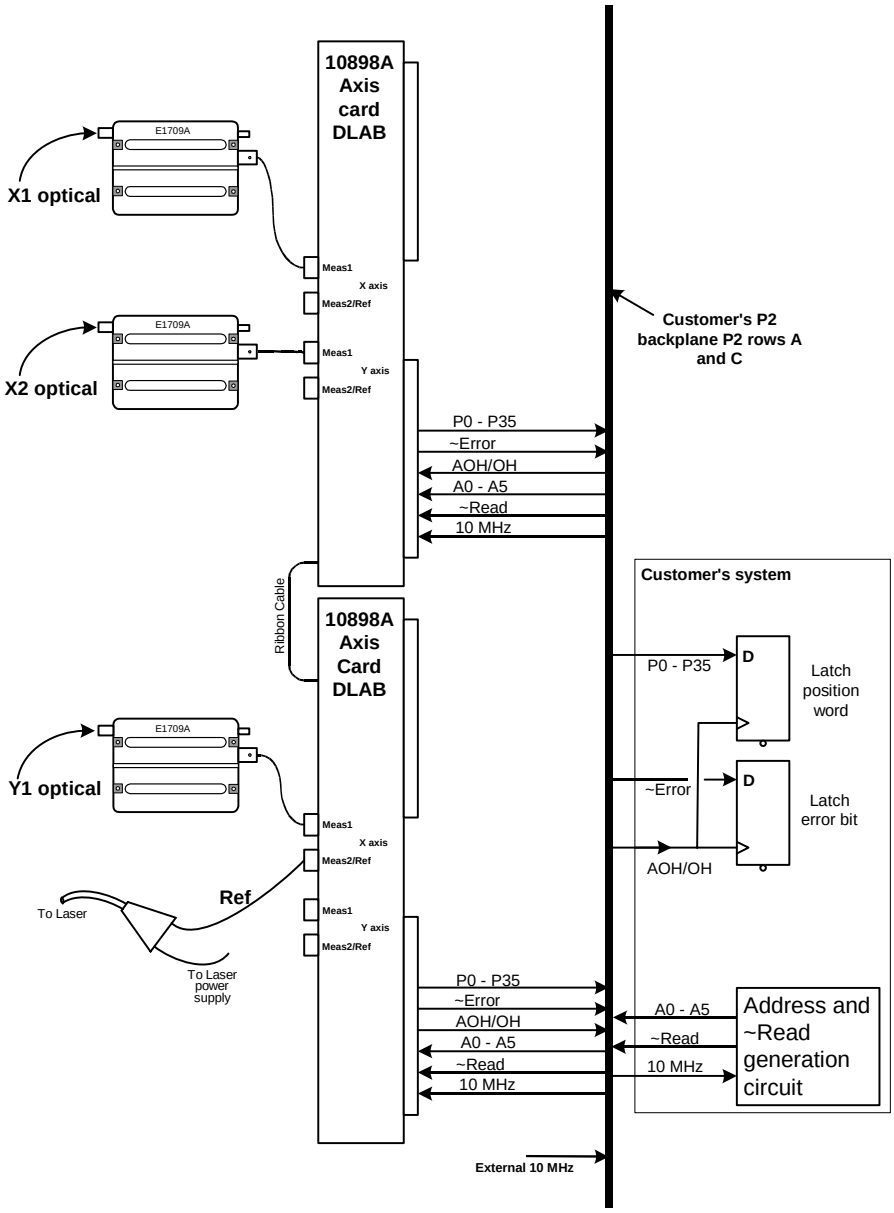


Figure 39 10898A electronics

The 10898A electronics shown in Figure 39 uses optical receivers to convert light from the optics to electrical square waves that are processed by the 10898A boards to determine position. To route the reference signal and power for the optical receivers between boards, a 16-pin ribbon cable is used.

In the N1225A based system, show in Figure 38, the optical receivers are integrated, so the fibers are routed directly from the optics to the board. No reference passing cable is shown in this diagram, since only one N1225A is used, but an Agilent provided reference cable is needed to allow two or more N1225As to share the same reference signal.

Considerations when replacing the 10897/8 boards with N1225A

- Take into account the difference in data age between the N1225A and 10897/8 boards
- The N1225A requires an optical reference
- P2 lines, ~Force zero, ~Sample, and Output hold, affect four axes per board
- P2 ~Position reset line can affect up to four axes
- The N1225A cannot accept a reference signal *from* the 10897/8 boards, or provide a reference *to* these boards.
- For a plane mirror application, the N1225A has four times the resolution of the 10897/8 boards. To maintain the same resolution at the P2 position outputs, set the Axis position alignment bits appropriately for each axis.
- Limits on the 10897A/B/C board hardware position output drive capability prevent this board from reliably driving P0–P35 if they have the standard VME termination. The N1225A and 10898A have adequate drive capability and high speed drivers so terminations are recommended. If resistive terminations are used, having the N1225A and 10897A/B/C driving the same P2 position lines will not be reliable.
- Software functions to accommodate the different register locations are needed. This is done by writing a new set of I/O functions or routines to access the N1225A registers instead of the 10897/8 board registers.

N1225A Diagnostic Functions

Refer to Chapter 7, “Maintenance and Service” for information on diagnostics.

N1225A Non-Linearity Correction (NLC) feature (Option 200)

Cyclic errors can be reduced significantly with Option 200. When enabled, cyclic error correction parameters (amplitude and phase) are learned, on the fly, and then these parameters are used to correct the measured position.

This option reduces cyclic error having a period of 1 fringe. The definition for a fringe depends upon the wavelength and the optics used. In the explanation below, 633nm and Plane Mirror optics (fold factor = 4) will be chosen as an example, so that real numbers can be included. For 633nm and Plane Mirror optics, 1 fringe = 158nm. While this option reduces cyclic error effectively most of the time, there are some limitations.

Start Up Limitation

When power is first applied, and stage motion begins, the stage must be moving above a minimum velocity of 0.158mm/sec and for a distance of 316nm (2 fringes) for the first correction parameters to be learned, after which position correction can begin.

Aliasing Velocity Windows Limitation

There are small “windows” of velocity where new correction parameters cannot be learned (or updated). We call these Aliasing Velocity Windows or Aliasing Velocities. If the stage velocity happens to momentarily be within one of these windows, the correction parameters are not updated. Instead, the output position continues to be corrected, using the correction parameters that were learned just before entering the aliasing window. After start up, as the stage velocity increases, the first aliasing velocity window occurs between 49.30mm/sec and 49.61mm/sec. While the velocity is within this window, new correction parameters are not updated, however position correction continues – using the parameters learned just before the stage velocity reached 49.30mm/sec. If the stage velocity has passed through this first aliasing window, and then slows down and enters the window again, the same situation occurs in that position correction continues, but using the parameters learned just before the stage reached 49.61mm/sec. The next aliasing velocity window occurs between 98.75mm/sec and 99.07mm/sec. Additional windows exist at multiples of 49.453mm/sec.

NOTE

The above limitations and the limits in the below table hold for + and – velocities (velocities in either direction). For linear optics, double the values in the table; divide them by 2 if using high resolution optics.

Table 7 Aliasing Velocity Range for plane mirror optics (mm/sec)

Minimum	Maximum
0.000	0.155
49.298	49.607
98.750	99.059
148.203	148.512
197.655	197.964
247.108	247.417
296.560	296.869
346.013	346.322
395.465	395.774
444.918	445.227
494.370	494.679
543.822	544.132
593.275	593.584
642.727	643.036
692.180	692.489
741.632	741.941
791.085	791.394
840.537	840.846
889.990	890.299
939.442	939.751
988.895	989.204

Amount of Cyclic Error Reduction

At this time, we believe that up to ± 8 nm of cyclic error is corrected (or reduced) to less than 1 nm, and sometimes to even much less than 1 nm; however, if the cyclic error is above ± 20 nm, no correction can occur.

4 Register Bit Descriptions

Introduction

This chapter provides an alphabetical list of all of the N1225A registers and describes the register contents in detail. Most of the registers repeat throughout the board's VME address space, so every $0200 there is another set. Some registers have bits that affect operation of the entire board. These registers are in the Axis1 addressing region (offsets $0000 through $01FF). If a bit only affects one axis its name is proceeded by AxisX to identify the axis to which the bit applies.

All offset values are on 32-bit boundaries. If using A16 addressing, be sure to add two to the offset value for registers where the data is in the least significant word.

Register Bit Description

The following sections list the registers and bits, and their operation, default values, address offsets, and reset values.

Undefined Register Bits

Writing zeros to undefined bits (shown as blanks in the register tables) of a register have no effect on product operations. Reading from undefined bits returns a zero.

Absolute Phase Registers

Axis 1 through 4 absolute phase registers

32-bit Offsets for Absolute Phase Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$0018	$0218	$0418	$0618

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Bit name	Description	Power Up or After Reset Value
B31 through B10	Read only bits, set to 0	N/A
B9 through B0	Read only bits, least significant bit represents {(2 * PI)/1024 = 6.1359} milliradians of (electrical) phase. Optically, for a plane mirror system, the lsb equals 1.534 milliradians of phase.	N/A

Board Gateway IP Address Register (32-Bit Offset $0050)

Two 32-bit registers hold the IPv4 gateway IP address using big endian format: IP[3].IP[2].IP[1].IP[0]

Offset	B15–B8	B7–B0
$0050	GIP[3]	GIP[2]
$0052	GIP[1]	GIP[0]

Board LAN Hostname Register (32-Bit Offset $00C0)

	B31-B24	B23-B16	B15-B8	B7-B0
$00C0	HOST[0]	HOST[1]	HOST[2]	HOST[3]
$00C4	HOST[4]	HOST[5]	HOST[6]	HOST[7]
$00C8	HOST[8]	HOST[9]	HOST[10]	HOST[11]
$00CC	HOST[12]	HOST[13]	HOST[14]	Null (0x00)

Bits	Name	Description	Power up or after reset value
B31–B24 B23–B16 B15–B8 B7–B0	HOST[0] through HOST[14]	The hostname string is stored as ASCII characters with the first character using bits B31 through B24 at address offset $00C0. Place a null character (0x00) at the end of the hostname string to terminate it. Max. of 15 characters in hostname with 16th character (HOST[15]) being null.	"an1225a-0000000" where 0000000 is the last 7 digits of the N1225A serial number

Board Level Diagnostics Register (32-Bit Offset $002C)

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0	+2.5 V O.K.	+1.2 V O.K.	+50 V O.K.	–12 V O.K.	+12 V O.K.	0	+3.3 V O.K.

Bit	Bit name	Description	Power Up or After Reset Value
B31–B7		Read only bits. Always read 0.	N/A
B6	+2.5 V O.K.	Read only bit. When set this bit indicates the internal +2.5 V supply of the N1225A is within its specified value. 0: outside specified voltage 1: within ±0.25 volts	N/A
B5	+1.2 V O.K.	Read only bit. When set this bit indicates the internal +1.2 V supply of the N1225A is within its specified value. 0: outside specified voltage 1: within ±0.12 volts	N/A
B4	+50 V O.K.	Read only bit. When set this bit indicates the internal +50 V supply of the N1225A is within its specified value. 0: outside specified voltage 1: within±5.0 volts	
B3	–12 V O.K.	Read only bit. When set this bit indicates the internal –12 V supply of the N1225A is within its specified value. 0: outside specified voltage 1: within ±1.2 volts	
B2	+12 V O.K.	Read only bit. When set this bit indicates the internal +12 V supply of the N1225A is within its specified value. 0: outside specified voltage 1: within ±1.2 volts	
B1		Read only bit Always reads zero.	
B0	+3.3 V O.K.	Read only bit. When set this bit indicates the internal +3.3 V supply of the N1225A is within its specified value. 0: outside specified voltage 1: within ±0.33 volts	

Board Level Error Status and Reset Register (32-Bit Offset $0028)

Bit	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
Channel	4	3	2	1	4	3	2	1	4	3	2	1	4	3	2	1
Error Condition	AC too high				DC too high				Below squelch				Loss of Lock			

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Axis	Reserved	Back-plane clock	Reference loss lock	Reference error bits	4	3	2	1	4	3	2	1	4	3	2	1
Error Condition	Reserved	Loss of Lock	Loss of Lock	Reference error	Position or velocity comparator bit				Position overflow				Data not valid			

Bit	Bit name	Description	Power Up or After Reset Value
B31 B30 B29 B28	Chan4 through Chan1 AC too high	Read/Write bit, latched, write “1” to this bit to clear it. 0: AC light power into channel, combined with APD gain setting is below clipping limit for photodiode amplifier (> 11468 or 70 µW). 1: Clipping is occurring or did occur since the last time this bit was reset.	0
B27 B26 B25 B24	Chan4 through Chan1 DC too high	Read/Write bit, latched, write “1” to this bit to clear it. 0: Total light power into channel, combined with APD gain setting is below clipping limit for photodiode amplifier (> 30719 or 187.5 µW). 1: Power level into channel is being exceeded or was exceeded since the last time this bit was reset.	0
B23 B22 B21 B20	Chan4 through Chan1 below squelch	Read/Write bit, latched, write “1” to this bit to clear it. 0: AC light power into channel is above the user defined squelch set-point in the respective channel's squelch setting register. 1: AC light power into channel fell below the user defined squelch set-point since the last time this bit was reset. Note: this will cause a channel loss of lock.	0
B19 B18 B17 B16	Chan4 through Chan1 loss of lock	Read/Write bit, latched, write “1” to this bit to clear it. 0: A channel loss of lock has not occurred since this bit was reset. 1: A channel loss of lock occurred. This will also cause a data invalid error that has to be reset.	0
B14	Backplane clock loss of lock	Read/Write bit, latched, write “1” to this bit to clear it. 0: Board clock synchronized with 10 MHz backplane clock (provided external clock is selected) 1: Board has lost synchronization with 10 MHz backplane clock since the last time this bit was reset.	0
B13	Reference Lost Lock	Read/Write bits, latched, write “1” to this bit to clear it. 0: no errors detected 1: reference lost lock detected	

B12	Reference error bits	Read/Write bits, latched, write “1” to this bit to clear it. 0: no errors detected 1: reference error detected	00
B11 B10 B9 B8	Axis4 though Axis1 position or velocity comparator bit	Read/Write bits, latched, write “1” to this bit to clear it. These bits are the ORed combination of the position and velocity comparator result bits for the respective axis. These bits represent the outcome of comparator operations specified by setting bits described in “Comparator Configuration Registers" on page 127. 0: false 1: true, indicates the set-points for the position and/or velocity comparators for this axis were reached since the last time this bit was reset.	N/A
B7 B6 B5 B4	Axis4 through Axis1 position overflow bit	Read/Write bits, latched, write “1” to this bit to this bit to clear it. 0: false 1: true, indicates that an axis position overflow occurred since the last time this bit was reset.	
B3 B2 B1 B0	Axis4 through Axis1 data not valid bit	Read/Write bits, latched, write “1” to this bit to clear it. These bits indicate a data value is suspect or invalid. See “Error Detection and Handling" on page 80 for more details about the data not valid bit. 0: data for this axis is valid. 1: true, an invalid or suspect data value occurred for this axis since the last time this bit was reset.	

Board Firmware/HW Revision Register (32-Bit Offset $0038)

This register contains hardware and firmware revision information for the board, expressed as “x.xx”. For example, rev A.01 would read 0x4101 hex and have the ASCII character 'A' in bits 15–8 and bits 7–0 contain the numbers “01”.

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
ASCII Major Version (hardware)								Minor Version (hardware)				Minor Version (hardware)			

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
ASCII Major Version (firmware)								Minor Version (firmware)				Minor Version (firmware)			

Bit Name	Description	Power Up or After Reset Value
B31 through B24	Read only. Major hardware version for product, specified as an ASCII character starting with ‘A’ (range ‘A’–’Z’).	N/A[1]
B23 through B20	Read only. Bits B23–B20 are the first numeral of the minor version number, expressed as a binary nibble.	N/A[1]
B19 through B16	Read only. Bits B19–B16 are the second numeral of the minor version number, expressed as a binary nibble.	N/A[1]
B15 through B8	Read only. Major version, specified as an ASCII character starting with 'A' (range 'A'–'Z').	N/A[2]
B7 through B4	Read only. Bits B7–B4 are the first numeral of the minor version number, expressed as a binary nibble.	N/A[2]
B3 through B0	Read only. Bits B3–B0 are the second numeral of the minor version number, expressed as a binary nibble.	N/A[2]

[1] Programmed at factory.
[2] Changes based on currently installed firmware.

Board Level Interrupt Vector Register (32-Bit Offset $0020)

The board has one interrupt vector, a 32-bit word offset of $0020. The Interrupt Vector register is loaded with the user-predefined interrupt vector value, to be asserted on the data bus during an interrupt acknowledge cycle. This register may also be read by a data transfer cycle.

The IRQ enable bit in the axis1 General Control and Status Register also has to be set to enable interrupts.

NOTE

Since it is an 8-bit register and data transfer cycles are D16 or D32 cycles, the upper bits B31 through B8 will be invalid during a data read cycle.

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0	Int vector bit7	Int vector bit6	Int vector bi5	Int vector bit4	Int vector bit3	Int vector bit2	Int vector bit1	Int vector bit0

Bit name	Description	Power Up or After Reset Value
B31 through B16	Read only bits, set to 0.Writing to these bits has no effect.	0
Interrupt vector bits 7 through 0	Read/Write bits used to set the interrupt vector for the board including axes 1 through 4. Interrupts for the board can be turned on/off using the board level IRQ mask register. The board level IRQ mask register bits determine which conditions in the board level error status and reset register can cause an interrupt to occur.	0

Board Level IRQ Error Mask Register (32-Bit Offset $00A4)

Bit	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
Channel	4	3	2	1	4	3	2	1	4	3	2	1	4	3	2	1
Error Condition	AC too high IRQ error mask bit				DC too high IRQ error mask bit				Below squelch IRQ error mask bit				Loss of lock IRQ error mask bit			

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Axis	Reserved	Back-plane 10MHz clock	Reference lost lock	Reference error	4	3	2	1	4	3	2	1	4	3	2	1
Error Condition	Reserved	Lost Lock IRQ error mask bit	Lost Lock IRQ Error Mask bit	Reference Error IRQ Error Mask bit	Position or velocity comparator bit IRQ error mask bit				Position overflow IRQ error mask bit				Data not valid IRQ error mask bit			

	Bit name	Description	Power up or after reset value
B31 B30 B29 B28	Chan4 through Chan1 AC too high IRQ Error Mask bit	Read/Write bits 0: No IRQ generated 1: Generate IRQ if AC light power into respective channel exceeds limit	0
B27 B26 B25 B24	Chan4 through Chan1 DC too high IRQ Error Mask bit	Read/Write bits 0: No IRQ generated 1: Generate IRQ if DC light power into respective channel exceeds limit	0
B23 B22 B21 B20	Chan4 through Chan1 below squelch IRQ Error Mask bit	Read/Write bits 0: No IRQ generated 1: Generate IRQ if AC light power into the channel falls below the user defined squelch set-point in the respective channel's squelch setting register	0
B19 B18 B17 B16	Chan4 through Chan1 loss of lock IRQ Error Mask bit	Read/Write bits 0: No IRQ generated 1: Generate IRQ if a loss of lock occurs on the respective channel	0
B15	reserved		
B14	Backplane clock loss of lock IRQ Error Mask bit	Read/Write bits 0: No IRQ generated 1: Generate IRQ if the board loses lock with the 10 MHz backplane	0

B13	Reference Lost Lock	IRQ Error Mask bit 0: No IRQ generated 1: Generate IRQ if Reference lost lock	0
B12	Reference Error IRQ Error Mask bit	0: No IRQ generated 1: Generate IRQ if Reference Error occurred.	
B11 B10 B9 B8	Axis4 though Axis1 position or velocity comparator bit IRQ Error Mask bit	Read/Write bits 0: No IRQ generated 1: Generate IRQ if position or velocity goes outside user defined limits	0
B7 B6 B5 B4	Axis4 through Axis1 position overflow bit IRQ Error Mask bit	Read/Write bits 0: No IRQ generated 1: Generate IRQ if Axis position overflow detected	0
B3 B2 B1 B0	Axis4 through Axis1 data not valid bit IRQ Error Mask bit	Read/Write bits 0: No IRQ generated 1: Generate IRQ if position value from the respective axis is invalid	0

Board Level Output Hold & Rate Control Register (32-Bit Offset $00B4)

In a multi-board configuration, a “master” board running in asynchronous mode 2 can drive the output hold (OH) line of the P2 bus at (10 MHz)/(N + 1) where “N” is a value set by the asynchronous mode 2 divisor bits. Customer-supplied equipment can use this signal and the 10 MHz backplane clock to synchronize sampling position over P2.

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
								Output hold line control		Async mode 2 divisor bit5	Async mode 2 divisor bit4	Async mode 2 divisor bit3	Async mode 2 divisor bit2	Async mode 2 divisor bit1	Async mode 2 divisor bit0

Bit	Bit name	Description	Power Up or After Reset Value
B7	Output hold line control	Refer to Figure 25 on page 73. 1: Causes the N1225A to drive the output hold line at (10 MHz)/(N + 1) where N = 0 to 63 and is set using the Async mode 2 divisor bits. (Note: this is opposite logic to output hold line enabling used in the 10898A) 0: Output hold line is not driven.	0
B5 B4 B3 B2 B1 B0	Async mode 2 divisor bits bit5 through bit0	Used to set the value of “N”.	0

NOTE

Do not drive the output hold line (B7 set to 1) if another board in the system is set to Async Mode 1, 2, or 3, or if this board is set to Async Mode 1 (see the Board Level Output Hold and Rate Control Register).

Board MAC Address Register (32-Bit Offset $0040)

Two 32-bit registers are used to hold the 12 character EUI-48 MAC address using 4 bits for each character. The MAC address is expressed as: MAC[5]: MAC[4]: MAC[3]: MAC[2]: MAC[1]: MAC[0], where each byte is used for two characters of the MAC address.

Offset	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
$0040	reserved								reserved							
$0042	MAC[5]								MAC[4]							
$0044	MAC[3]								MAC[2]							
$0046	MAC[1]								MAC[0]							

Board Reference Error Register (32-Bit Offset $0058)

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0	0	Return clock lost status bit	Early clock lost status bit	Passed ref channel AC power too high	Passed ref channel DC power too high	Passed ref channel below squelch	Passed ref channel loss of lock

Bit	Bit Name	Description	Power up or after reset value
B31 through B6		Read only bits, set to 0	0
B5	Return clock lost status bit	Read/write bit, latched. 0: the "return clock" is present at this board. 1: return clock signal is not present This status bit can be cleared by writing "1" to it, or writing "1" to bit 12 of the Board Level Error Status and Reset Register (BLESRR) at offset 0x002A. This bit does not affect any bits in the BLESRR. The return clock is a clock signal passed in the reverse direction over the reference passing cable from the next board downstream in the reference passing chain. For the last slave board, this bit is always set and cannot be cleared. This bit is only concerned with the clock and not with the reference signal source.	N/A
B4	Early clock lost status bit	Read/write bit, latched. 0: the "early clock" is present at this board. 1: early clock signal is not present This status bit can be cleared by writing "1" to it, or writing "1" to bit 12 of the Board Level Error Status and Reset Register (BLESRR) at offset 0x002A. The "early clock" is a clock signal from the previous board in the reference passing chain. For a master board, this bit is always "0". This bit is only concerned with the clock and not with the reference signal source.	N/A
B3	Passed ref channel AC power too high	Read/write bit, latched, write 1 to clear* 0: AC power into the reference channel of the master board has remained below the maximum power specification since the last time this bit was reset. 1: AC power into the reference channel has exceeded the maximum power level specification at some time since this bit was reset.	N/A

Bit	Bit Name	Description	Power up or after reset value
B2	Passed ref channel DC power too high	Read/write bit, latched, write 1 to clear* 0: DC power into the reference channel of the master board has remained below the maximum power specification since the last time this bit was reset. 1: DC power into the reference channel has exceeded the maximum power level specification at some time since this bit was reset.	N/A
B1	Passed ref channel below squelch	Read/write bit, latched, latched, write 1 to clear* 0: AC power into the reference channel of the master board has remained above the squelch setting since the last time this bit was reset. 1: AC power into the reference channel has fallen below the squlch setting since the last time this bit was reset.	N/A
B0	Passed ref channel loss of lock	Read/write bit, latched, latched, write 1 to clear* 0: The reference channel of the master board has remained locked since the last time this bit was reset. 1: The reference channel of the master board fell out of lock since the last time this bit was reset.	N/A

* The error bit must be cleared on the master board before it can be cleared on the slave boards.

If any of these reference error bits are set, the reference error bit in the Board level error and status register will be set. In addition, all axes that depend on the reference channel will have their “data not valid” bit set in the Board level error and status register.

To clear these error bits, write “1” to them, or write “1” to the Reference error bit in the Board level error and status register.

NOTE The reference error propagates to all the boards in the reference chain, so be sure to clear the reference error on all the boards.

Board Reference ID Register (Offset $0010)

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
												Ref ID bit 3	Ref ID bit 2	Ref ID bit 1	Ref ID bit 0

Bit	Bit name	Description	Power Up or After Reset Value
B3 B2 B1 B0	Reference ID bits	Read only bits. When the reference cable is used to connect boards together, these four bits indicate the location of the board in the reference passing daisy chain, starting with 0x0 for the master board and counting up for each successive board in the chain.	Depends on system configuration

Board Serial Number Register (32-Bit Offset $02C0)

The board serial number register holds 15 ASCII characters, which accommodates the 10 character, null terminated serial number. There are four characters per 32-bit register starting with address offset $02C0.

Serial number format: “US12345678” with the first character, “U”, located in bits 31–24 at address offset $02C0 and terminated with a null character at bits 15–8 at $02C8.

	Bits 31–24	Bits 23–16	Bits 15–8	Bits 7–0
$02C0	1st character	2nd	3rd	4th
$02C4	5th	6th	7th	8th
$02C8	9th	10th	null character	null character
$02CC	null character	null character	null character	null character

Bits	Name	Description	Power up or after reset value
B31–B24 B23–B16 B15–B8 B7–B0	SerialNum[0] through SerialNum[15]	The serial number string is stored as 10 ASCII characters with the first character using bits B31 through B24 at address offset $02C0	Programmed at factory

Channel Status/Diagnostics Register (32-Bit Offset $003C)

32-bit Offsets for Channel/Diagnostics Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$003C	$023C	$043C	$063C

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
D15	D14	APD temp bit13	APD temp bit12	APD temp bit11	APD temp bit10	APD temp bit9	APD temp bit8	APD temp bit7	APD temp bit6	APD temp bit5	APD temp bit4	APD temp bit3	APD temp bit2	APD temp bit1	APD temp bit0

Bit	Bit name	Description	Power Up or After Reset Value
B13 through B0	APD temp bit13 through bit0	Read only. Indicates temperature in the area of the avalanche photodiode (APD). lsb is 7.61 m° C.	N/A

Command Registers

32-bit Offsets for Command Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$000C	$020C	$040C	$060C

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	All axes reset bit[a]	Sample AxisX absolute phase	Drive sample 4*	Drive sample 3[a]	Drive sample 2[a]	Drive sample 1[a]	AxisX posit-i on reset	AxisX sample vel2	AxisX sample vel1	AxisX sample pos6	AxisX sample pos5	AxisX sample pos4	AxisX sample pos3	AxisX sample pos2	AxisX sample pos1

* These bits are only in the Axis1 command register.

NOTE

The Command register is a write-only register. Bits listed that are set in the value written to the Command register through VMEbus will cause an immediate action.

Bit	Bit name	Description	Power Up or After Reset Value
B14	All axes reset bit	Write only. 1: Writing “1” simultaneously resets or presets all four axes. 0: Writing “0” has no effect.	N/A
B13	Sample AxisX absolute phase	Write only. Any number of bits can be written at one time. 1: Writing “1” causes the absolute phase of the axis to be written to the absolute phase register. 0: Writing “0” has no effect.	N/A
 B12 B11 B10 B9	Axis1 only Drive sample4 Drive sample3 Drive sample2 Drive sample1	Write only. These bits are only in the Axis1 command register. 1: Writing a “1” causes the corresponding ~Sample4 through ~Sample1 line on the P2 backplane to be brought low for 100 ns synchronous with the backplane 10 MHz clock. Useful for initiating a simultaneous sample by all axes on this board and other boards in the backplane. 0: Writing “0” has no effect.	N/A
B8	AxisX position reset	Write only. 1: Sets the axis position to 0 if the preset enable bit in the axis general control and status register is 0. Sets axis position to value in the axis position offset register if the preset enable bit = 1. 0: Writing “0” has no effect.	N/A

B7 B6	AxisX sample velocity2 sample velocity1	Write only. Any number of bits can be written at one time. 1: Writing “1” causes the axis velocity to be written to the respective axis velocity registers. 0: Writing “0” has no effect.	N/A
B5 B4 B3 B2 B1 B0	AxisX Sample position6 Sample position5 Sample position4 Sample position3 Sample position2 Sample position1	Write only. Any number of bits can be written at one time. 1: Writing “1” causes the axis position to be written to the respective axis position registers. 0: Writing “0” has no effect.	N/A

Register bits are described in the following sections.

Drive Sample1 to Drive Sample4

Writing one or more of these bits will generate a ~Sample pulse that is synchronous with the 10 MHz clock. This pulse will sample all axes of the laser axis board and will appear as an output on the corresponding ~Sample1 to ~Sample4 pin of the P2 connector. This allows one board to cause sampling to occur on other boards in the rack.

Reset Position

Writing this bit will reset the Position Counter according to the state of the Preset Enable bit in the General Control & Status register. See “General Control and Status Register" on page 135.

Sample Position1 to Sample Velocity2

Writing one or more of these bits transfers the current contents of the Position Counter to one or more of the six Position registers or two Velocity registers.

Any combination of commands may be executed with a single write to the Command register. Writing a value of zero does nothing.

Comparator Configuration Registers

The comparator registers provide set-points, these registers set what test is performed. Comparator “A” is the lower limit, comparator “B” is the upper limit.

32-bit Offsets for Comparator Configuration Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$007C	$027C	$047C	$067C

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
		AxisX Bd level err reg comp output bit select bit1	AxisX Bd level err reg comp output bit select bit0	AxisX vel comp latched result	AxisX vel comp realtime result	AxisX vel comp result config bit1	AxisX vel comp result config bit0		AxisX vel compB test bit2	AxisX vel compB test bit1	AxisX vel compB test bit0		AxisX vel comp A test bit2	AxisX vel comp A test bit1	AxisX vel comp A test bit0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
All axes row comp and error output enable *	Axis D row comp-arator config bit2	Axis D row comp-arator config bit1	Axis D row comp-arator config bit0	AxisX pos comp latched result	AxisX pos comp realtime result	AxisX pos comp result config bit1	AxisX pos comp result config bit0		AxisX pos compB test bit2	AxisX pos compB test bit1	AxisX pos compB test bit0		AxisX pos comp A test bit2	AxisX pos comp A test bit1	AxisX pos comp A test bit0

* This bit is present only in the Axis1 register.

The N1225A comparators can be set to initiate taking data when position and (optionally) velocity shown by the curved line are within limits “A” and “B” as shown in Figure 40. The comparator can be configured to trigger when position or velocity is below the value “A” as in region I, or between “A” and “B” (regions II and IV), or above the value “B” as in region III.

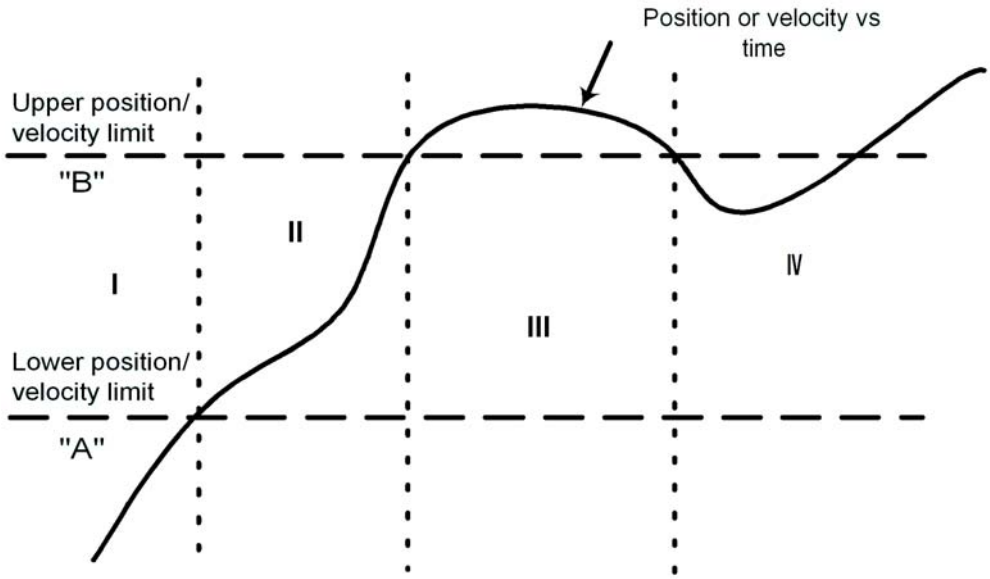


Figure 40 Graphical view of comparator limits

Bit	Bit name	Description	Power Up or After Reset Value
B29 B28	AxisX board level error register comparator output bit select bit1, bit0	Read/Write bit. The board level error status and reset register (see "Board Level Error Status and Reset Register (32-Bit Offset $0028)" on page 112) has one bit per axis for axis comparator results, and latches the result. Bits B28 and B29 determine which comparator result appears in this register. 00: disabled (output bit stays at 0). 01: real time bit in board level error register for this axis is result of velocity comparator logic. 10: real time bit reflects position comparator logic. 11: latched bit reflects the ORed result of both position and velocity comparisons.	00
B27	AxisX velocity comparator latched result	Read/Write. Write "1" to reset bit. 0: Indicates velocity comparator limits have not been reached since this bit was reset. 1: Velocity comparator limits met since last time bit was reset.	N/A
B26	AxisX velocity comparator realtime result	Read only. Writing to this bit has no effect. This bit indicates a "real time" condition. 0: Indicates velocity comparator limits are not currently being met. 1: Velocity comparator limits are being met.	N/A

Bit	Bit name	Description	Power Up or After Reset Value
B25 B24	AxisX vel comp result config bits bit1, bit0	Read/Write. Bit settings and test performed. 00: Comparison #1 true AND Comparison #2 true. 01: Comparison #1 true OR Comparison #2 true. 10: Comparison #1 true AND Comparison #2 false. 11: Comparison #1 false AND Comparison #2 true.	N/A
B22 B21 B20	AxisX vel compB test bits bit2, bit1, bit0	Read/Write. These bits determine what is a “true” or “false” condition when comparing AxisX velocity with the value loaded into the velCompB1 register. This is “Comparison #2”. 000: AxisX velocity > velCompBX. 010: AxisX velocity <= velCompBX.	000
B18 B17 B16	AxisX vel compA test bits bit2, bit1, bit0	Read/Write. These bits determine what is a “true” or “false” condition when comparing Axis1 velocity with the value loaded into the velCompA1 register. This is “Comparison #1”. 000: Axis1 velocity > velCompAX. 010: Axis1 velocity <= velCompAX.	000
B15	Output enable for D row hardware comparator and error outputs (all)	Enable bit for hardware comparator output on D row and D row error output (enables/disables D row error and comparator outputs for all axes). 0: Hardware comparator and error output disabled. 1: Hardware comparator and error output enabled.	0
B14 B13 B12	Axis D row comparator output configuration bits bit2 bit1 bit0	Read/Write bits. These bits control the output mode for the Axis comparator output pin on the D row of P2 for the respective axes. They are a copy of the result bits in the comparator configuration register. Note: the D row comparator outputs are bussed and cannot be disabled individually. Note These pins are used for the position comparator or the velocity comparator output. 000 velocity, real time, TTL low 001 velocity, real time, TTL high 010 position, real time, TTL low 011 position, real time, TTL high 100 velocity, latched, TTL low 101 velocity, latched, TTL high 110 position, latched, TTL low 111 position, latched, TTL high	000
B11	Axis1 position comparator latched result	Read/Write. Write “1” to reset bit. 0: Indicates position comparator limits have not been reached since this bit was reset. 1: Position comparator limits met since last time bit was reset.	N/A
B10	AxisX position comparator real time result	Read only. Writing to this bit has no effect. This bit indicates a “real time” condition. 0: Indicates position comparator limits are not currently being met. 1: Position comparator limits are being met.	N/A

Bit	Bit name	Description	Power Up or After Reset Value
B9 B8	AxisX pos comp result config bits bit1, bit0	Read/Write. Bit settings and test performed. 00: Comparison #1 true AND Comparison #2 true. 01: Comparison #1 true OR Comparison #2 true. 10 Comparison #1 true AND Comparison #2 false. 11 Comparison #1 false AND Comparison #2 true.	00
B6 B5 B4	AxisX pos compB test bits bit2, bit1, bit0	Read/Write. These bits determine what is a “true” or “false” condition when comparing Axis1 position with the value loaded into the compB register. This is “Comparison #2”. 000: AxisX position > CompB. 010: AxisX position <= CompB.	000
B2 B1 B0	AxisX pos compA test bits bit2, bit1, bit0	Read/Write. These bits determine what is a “true” or “false” condition when comparing Axis1 position with the value loaded into the compA register. This is “Comparison #1”. 000: AxisX position > CompA. 010: AxisX position <= CompA.	000

Filter Control Registers

Each axis has these registers, which are used to low pass filter the position data before it goes to the P2 connector (including position data read from D and Z rows) with Kp and Kv used to select filter constants.

The filter is always in the measurement path and the default value of $0000 corresponds to K_p of 2^{-8} and Kv of 2^{-14} which is a relatively slow response. Selecting K_p of 2^{-5} and Kv of 2^{-11} provides the fastest response.

32-bit Offsets for Filter Control Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$00B8	$02B8	$04B8	$06B8

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
reserved															

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
												K_{p1}	K_{p0}	K_{v1}	K_{v0}

Bit	Bit name	Description	Power Up or After Reset Value
B31–B16	reserved	These bits read zero	0
B15–B4		These bits read zero	0
B3	K_{p1}	Read/Write bit	0
B2	K_{p0}	Read/Write bit	0
B1	K_{v1}	Read/Write bit	0
B0	K_{v0}	Read/Write bit	0

Table 8 shows the values of K_p and K_v used in the filter, and corresponding to values of K_{p1}, K_{p0}, K_{v1} and K_{v0}. Figures 41 and 42 show the filter time response using a plot of following error for a 100 g acceleration. Time along the horizontal axis is in units of 100 ns, so a value of 300 corresponds to 3 µs.

Only use combinations of K_p and K_v values in the table below, other values will result in unstable position readings.

Table 8 Filter Constants

Bits B15–B0	K_p Value	K_v Value	Following Error	Comments
$0000	2^{-8}	2^{-14}	1.6 nm/g	
$0004	2^{-7}	2^{-14}	1.6 nm/g	
$0008	2^{-6}	2^{-14}	1.6 nm/g	
$000C	2^{-5}	2^{-14}	1.6 nm/g	
$0001	2^{-8}	2^{-13}	0.8 nm/g	
$0005	2^{-7}	2^{-13}	0.8 nm/g	
$0009	2^{-6}	2^{-13}	0.8 nm/g	
$000D	2^{-5}	2^{-13}	0.8 nm/g	
$0002	2^{-8}	2^{-12}	0.4 nm/g	Not recommended
$0006	2^{-7}	2^{-12}	0.4 nm/g	
$000A	2^{-6}	2^{-12}	0.4 nm/g	
$000E	2^{-5}	2^{-12}	0.4 nm/g	
$0003	2^{-8}	2^{-11}	0.2 nm/g	Not recommended
$0007	2^{-7}	2^{-11}	0.2 nm/g	Not recommended
$000B	2^{-6}	2^{-11}	0.2 nm/g	
$000F	2^{-5}	2^{-11}	0.2 nm/g	

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NOTE

Whenever filter settings or the Laser Source Control Register contents are changed, you must reset (or preset) the axis that's affected, then wait a minimum of 100 µs to allow the filter to settle. Resetting (or presetting) the axis initializes the filter.

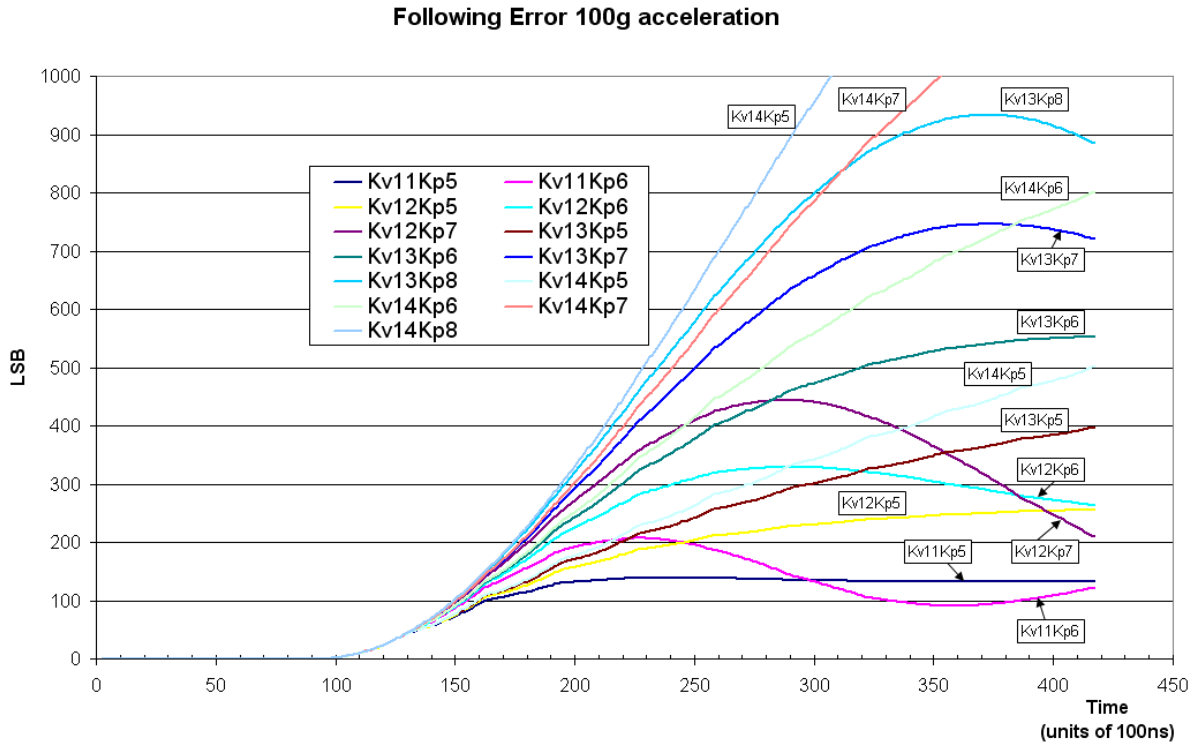


Figure 41 Expanded view of initial filter response to 100g acceleration

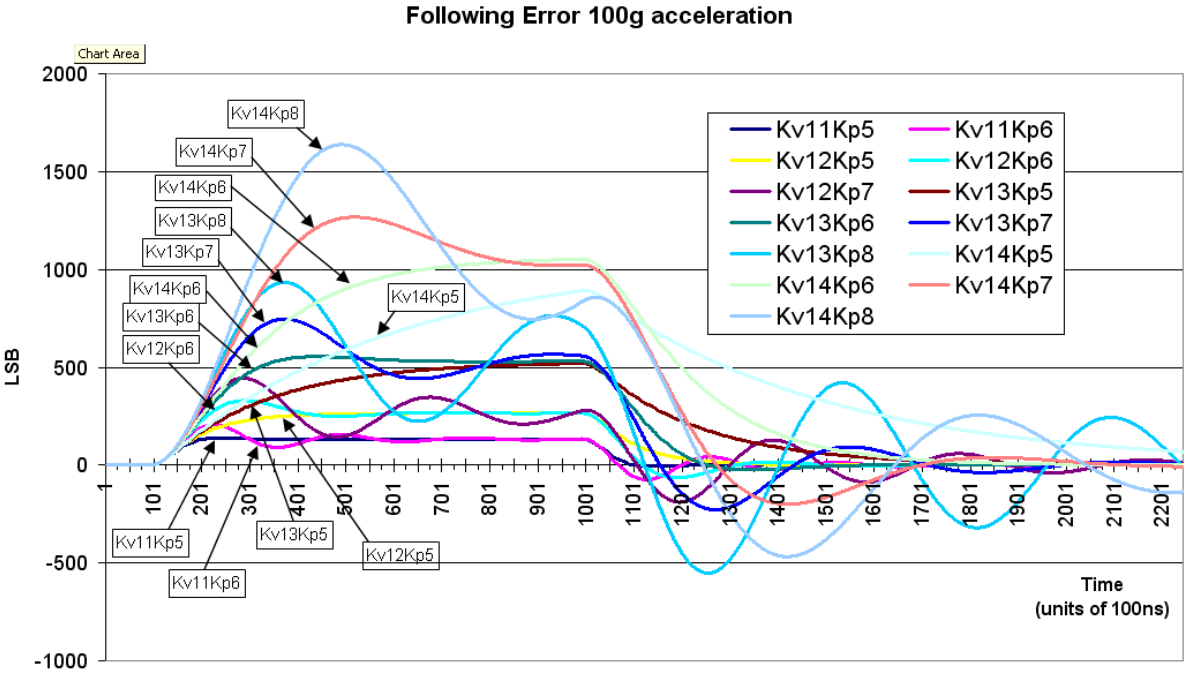


Figure 42 Filter response to 100g acceleration

Gain and Squelch Settings Registers

Channels 1 through 4 gain and squelch settings

32-bit Offsets for Gain and Squelch Settings Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$001C	$021C	$041C	$061C

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
reserved											APD gain setting bit4	APD gain setting bit3	APD gain setting bit2	APD gain setting bit1	APD gain setting bit0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Bit name	Description	Power Up or After Reset Value
APD gain bits B20 through B16	Read/Write bits 00000: AGC on 00001: AGC off, APD set to low gain (M4) 00010: AGC off, APD set to medium gain (M10) 00011: AGC off, APD set to medium-high gain (M20) 00100: AGC off, APD set to high gain (M50)	00000
Squelch setting, bits B15 through B0	Read/Write bits set by user. If channel AC power level falls below this setting, a channel loss of lock error and data invalid error will occur and latch. This will require resetting lsb = (200 µW/32767) = 0.0061µW	0

General Control and Status Register

The bits of the General Control & Status Register are defined as shown in the second table below. Bits 0 through 9 are read/write and are used for control; bits 10 through 15 are read only and reflect status.

32-Bit Offsets for General Control and Status Register	Axis 1	Axis 2	Axis 3	Axis 4
	$0000	$0200	$0400	$0600

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	ChanX High Temp	AxisX SigA	AxisX SigB		AxisX Samp Pend	AxisX Pos Reset Disable	AxisX Force zero Disable	System LED*	AxisX Preset Enable	HW Samp Mode 1*	HW Samp Mode 0*	Board Level IRQ Enable*	Intr Level bit 2*	Intr Level bit 1*	Intr Level bit 0*

* These bits are only in the Axis1 General Control and Status Register.

Axis1 General Control and Status Register

Bit	Bit name	Description	Power Up or After Reset Value
B14	ChanX High Temp	Read only, real time bit Each channel has its own temperature monitor located in the photodiode amplifier section. 0: temperature is below 55° C 1: temperature exceeds 55° C	Depends on board temperature
B13 B12	AxisX SigA AxisX SigB	Read only, real-time bit Signal A and Signal B refer to the inputs used to compute position for each axis (selected using the Laser source control register). The SigA and SigB bits are true if the respective signals are present. 0: signal is not present 1: signal is present Note: There are some special channel settings for test purposes.	Depends on presence of SigA & SigB
B10	AxisX samp pend	Read only, real-time bit Sample pending. Indicates that a register identified in the Sample Mode and Mask register contains a position or velocity value to read.	0
B9	AxisX pos reset disable	Read/Write bit This bit controls what occurs when the ~Position Reset input (P2-A7) is brought low. 0: position counter on this axis will be reset 1: this axis will not be reset when the ~Position Reset input (P2-A7) is brought low Note: See “preset enable” bit below for information on what “reset” means.	1

Axis1 General Control and Status Register (continued)

Bit	Bit name	Description	Power Up or After Reset Value
B8	AxisX Force zero disable	Read/Write bit. This bit controls zeroing of the position outputs for this axis when the hardware ~Force zero Reset input (P2-A6) is brought low. Stored position value is not affected. 0: the hardware position register will be zeroed. 1: this axis hardware position register will not be set to zero when ~Force zero is brought low.	0
B7	System LED	Read/Write bit. After the board has booted, the status LED is under user control and if the boot process was successful, the LED will be on continuously (green). If an unrecoverable error occurs, the status LED will go off. 0: changes the status LED color to green. 1: changes the status LED to amber.	0
B6	AxisX preset enable	Read/Write bit. This bit controls what gets written to the position counter during a position reset (affects resets using hardware (P2-A7 pin) or VMEbus). 0: position counter is zeroed. 1: the position offset register contents are loaded into the position counter.	0
B5	HW samp mode 1	The two hardware sample mode bits affect where the position and velocity values are written when the P2 bus hardware ~Sample1 and ~Sample2 lines are brought low. The samp mode 0 bit is associated with the ~Sample1 line and the samp mode 1 bit works with ~Sample2. All axes on the board are affected. 1: If the HW samp mode 1 bit is set and the ~Sample2 line is brought low, then position and velocity for each axis will be written to their respective Position2 and Velocity2 registers. 0: If the HW samp mode 0 bit is cleared, then only the position is written to the Position1 register of all axes.	0
B4	HW samp mode 0	The two hardware sample mode bits affect where the position and velocity values are written when the P2 bus hardware ~Sample1 and ~Sample2 lines are brought low. The samp mode 0 bit is associated with the ~Sample1 line and the samp mode 1 bit works with ~Sample2. All axes on the board are affected. 1: If the HW samp mode 0 bit is set and the ~Sample1 line is brought low, then position and velocity for each axis will be written to their respective Position1 and Velocity1 registers. 0: If the HW samp mode 0 bit is cleared, then only the position is written to the Position1 register of all axes.	0
B3	Board level IRQ enable	Enables interrupts for board. 0: interrupts not enabled 1: interrupts enabled	0
B2 B1 B0	Intr level bit 2 Intr level bit 1 Intr level bit 0	If interrupts are enabled (IRQ enable bit set), these bits set the interrupt priority from 1 to 7. Intr level bit 0 is the lsb.	0

IP Address Register (32-Bit Offset $0048)

Two 32-bit registers are used to hold the IPv4 address using 8 bits for each value in the dot address, for example:

IP[3].IP[2].IP[1].IP[0]

Offset	B15–B8	B7 –B0
$0048	IP[3]	IP[2]
$004A	IP[1]	IP[0]

The IP address will be supplied via DHCP when DHCP is selected, so no default value is provided.

Access: Read/Write

LAN Status/Configuration Register (32-Bit Offset $0054)

Bits 31 through 16 constitute the LAN Status register part of this 32-bit register and reflect completed actions directed by writing bits to and from the LAN Configuration register portion (bits 15 through 0).

Offset	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
$0054								LAN active	reserved			Static IP accepted	reserved	DHCP renewed	DHCP released	DHCP enabled

Offset	B15	B14	B13	B12	B11	B10	B9	B8	B7–B5	B4	B3	B2	B1	B0
$0056								Host name accept	reserved	Static IP accept	reserved	DHCP renew	DHCP release	DHCP enable

Bit	Bit name	Description	Power Up or After Reset Value
B24	LAN active	Read only 0: LAN is inactive 1: LAN is active	
B20	Static IP accepted	Read only 0: pending 1: accepted	
B18	DHCP renewed	Read only 0: pending 1: renewed	
B17	DHCP released	Read only 0: pending 1: released	
B16	DHCP enabled	Read only 0: pending/disabled 1: enabled	N/A

NOTE

Bits 0 and 4 are mutually exclusive. If DHCP is enabled, IP Address through Gateway IP registers are read only. If Static IP is accepted, the mentioned registers will have R/W access.

Bit	Bit name	Description	Power Up or After Reset Value
B8	Hostname accept	Write only): no effect 1: Issues a command to the board to use the Hostname register After updating the Hostname register, writing "1" to this bit commands the board to accept the new hostname.	
B4	Static IP accept	Write only 0: no effect 1: command to accept Setting this bit requests that Static IP addressing be set for the N1225A. When this request has been completed the Static IP accepted bit is set. See previous table.	N/A
B2	DHCP renew	Write only 0: no effect 1: command to renew Setting this bit causes the board to release the current DHCP lease and then renew the lease. This process obtains new DHCP settings from any available server on the network. In order for this to work, the board must be in DHCP mode.	N/A
B1	DHCP release	Write only 0: no effect 1: command to renew Setting this bit causes the board to release the current DHCP lease, allowing the server to recover the IP address of the board for re-use. When this occurs the IP address of the board is set to the default, 0.0.0.0. In order for this to work, the board must be in DHCP mode.	N/A
B0	DHCP enable	Write only 0: no effect 1: command to enable DHCP Setting this bit requests that DHCP mode be set for the N1225A, and static IP addressing be deselected. When this request completes, the DHCP enabled bit, B16, is set. See above.	N/A

NOTE

Bits 0 and 4 are mutually exclusive. The last write will determine the final value, with DHCP having priority if both are set. Setting a bit in the configuration register automatically clears the corresponding bit in the status register. Be sure to poll the LAN status register to see if command has been processed. The LAN configuration is stored in memory and restored when board power is reapplied.

When DHCP is selected, the contents of the IP, GIP (Gateway IP), and SNM (Subnet Mask) registers are not updated until the DHCP enabled bits and DHCP renewed bits are high in the LAN Status Register. These status bits are updated when a lease from a DHCP server is received. If the Ethernet cable is

unconnected, or the DNS server is not present, the wait could be forever. Typically, the DHCP transactions, discover to lease grant, occur within ten seconds when the DHCP server is not busy and network traffic is low.

With static IP, the setup is shorter because the N1225A does not have to wait for an external DHCP server but many things can affect the wait time before the LAN registers can be accessed. For example, the EEPROM is updated, which takes no more than 1 ms, but the microprocessor could also be responding to Ethernet traffic from a previous configured state, route table setups, or other software related tasks therefore the time is variable and difficult to predict.

Here is what to expect during boot-up:

DHCP at boot time (no configuring)

1 The front panel LED becomes green and the firmware revision/version registers have values other than zero. The board is fully functional as a laser axis board at this time.

2 The MAC Address register is updated.

3 The DHCP requests are transmitted. The LAN Status register indicates DHCP

4 The DHCP leases are obtained.

5 The IP, GIP, SNM, and maybe hostname, are updated.

6 The LAN Status register indicates DHCP renewed.

Static IP at boot time (no configuring)

1 The front panel LED becomes green and the firmware revision/version registers have values other than zero. The board is fully functional as a laser axis board at this time.

2 The MAC Address register is updated. The LAN Status register indicates only the LAN is active.

3 The IP, GIP, SNM, and hostname are copied from EEPROM.

4 The LAN Status register indicates the Static IP has been accepted.

With either of these configurations, the corresponding indicators in the LAN Status register will signal when they are done with the work. Here are some simple procedures for DHCP and static IP assuming the board has already booted.

DHCP procedure

1. Set the DHCP Enable bit in the LAN Configuration register.
2. Wait for the DHCP Renewed and the DHCP Enabled bits to be true in the LAN Status register.
3. If ten seconds elapse and the LAN Active bit is set in the LAN Status register, there are problems with the network. Retry or fail.

Static IP procedure

1. The Static IP Accepted bit in the LAN Status register should be true if previous configuration is static IP (especially after boot).
2. Write the desired IP, GIP, SNM, and hostname registers.
3. Set the Static IP Accept bit in the LAN Configuration register.
4. Wait for the Static IP Accepted bit in the LAN Status register. This will occur within five seconds.

Laser Source Control Register

32-Bit Offsets for Laser Source and Control Register	Axis 1	Axis 2	Axis 3	Axis 4
	$0004	$0204	$0404	$0604

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
							AxisX dir sense	AxisX MeasA Select3	AxisX MeasA Select2	AxisX MeasA Select1	AxisX MeasA Select0	AxisX MeasB Select3	AxisX MeasB Select2	AxisX MeasB Select1	AxisX MeasB Select0

Bit	Bit name	Description	Power Up or After Reset Value
B8	AxisX dir sense	If AxisX dir sense bit = 0 then the AxisX position counter counts up when the measure freq >ref freq. By default, the “A” channel input is considered the “measure” input and “B” is the “reference”. See MeasA and MeasB select bits below. Clearly, the choice of which input is assigned for MeasA and MeasB will affect whether position counter counts increase or decrease as the stage is moved.	0

Bit	Bit name	Description	Power Up or After Reset Value
B7 B6 B5 B4	AxisX MeasA Select3 AxisX MeasA Select2 AxisX MeasA Select1 AxisX MeasA Select0	Position is measured by tracking the phase difference between the reference and measure signal inputs (computing "A - B"). The MeasA bits select the "A" source (nominally the measure input). Select0 is the lsb. 0000Channel 1 0001Channel 2 0010Channel 3 0011 Channel 4 0100Electrical reference from adjacent board 0101Simulates a channel whose phase value is always 0. It also will make the "SigA" bit in the general control and status register =1, permitting clearing errors for test purposes 0110 through 1111 phase for the selected Meas channel and "SigA" bit will be 0.	0000
B3 B2 B1 B0	AxisX MeasB Select3 AxisX MeasB Select2 AxisX MeasB Select1 AxisX MeasB Select0	Position is measured by tracking the phase difference between the reference and measure signal inputs (computing "A - B"). The MeasB bits select the "B" source (nominally the measure input). Select0 is the lsb. 0000Channel 1 0001Channel 2 0010Channel 3 0011Channel 4 0100Electrical reference from adjacent board 0101Simulates a channel whose phase value is always 0. It also will make the "SigB" bit in the general control and status register =1, permitting clearing errors for test purposes 0110 through 1111 phase for the selected Meas channel and "SigB" bit will be 0.	0011

Default Power-Up and Reset Values

Bit	Bit name	Axis1 Power Up or After Reset Value	Axis2 Power Up or After Reset Value	Axis3 Power Up or After Reset Value	Axis4 Power Up or After Reset Value
B8	AxisX dir sense	0	0	0	0
B7 B6 B5 B4	AxisX MeasA Select3 AxisX MeasA Select2 AxisX MeasA Select1 AxisX MeasA Select0	0000	0001	0010	0011
B3 B2 B1 B0	AxisX MeasB Select3 AxisX MeasB Select2 AxisX MeasB Select1 AxisX MeasB Select0	0011	0011	0011	0011

NLC Flag & Phase/Magnitude Correction Registers

These registers hold the phase and magnitude values applied to the respective axes to correct for first order cyclic error as described in Chapter 3, in the section "N1225A Non-Linearity Correction (NLC) feature (Option 200)" on page 102. These registers also hold a bit that indicates whether new NLC values are being computed.

32-bit Offsets for Non-Linearity Compensation Phase/ Magnitude Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$00E0	$02E0	$04E0	$06E0

.

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
NLC Qualified	0	0	0	NLC Phase Corrections											

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
NLC Magnitude Correction															

Bit	Bit Name	Description	Power up or after reset value
B31	NLC Qualified	Read only. 1: Valid Non-Linearity Correction (NLC) values are or can be computed for the present conditions of axis velocity 0: new NLC values are not being computed (albeit the previously computed values will be applied to the current measurement, provided that NLC is enabled for the respective axis.	0
B30 through B28	0	Read only. These bits always read 0	0
B27 through B16	NLC Phase Correction	Read only. This is phase of first order cyclical error. LSB = 2π/4096	N/A
B15 through B0	NLC Magnitude Correction	Read only. LSB = (laser wavelength) / [(fold factor) * 1024]	N/A

Output Control and Status Register

32-Bit Offsets for Output Control and Status Register	Axis 1	Axis 2	Axis 3	Axis 4
	$0008	$0208	$0408	$0608

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Board level clock mode select1*	Board level clock mode select0*	Async mode select1*	Async mode select0*	AxisX P2 bus bit align 1	AxisX P2 bus bit align 0	AxisX P2 bus addr bit A5	AxisX P2 bus addr bit A4	Board level Error mode select2*	Board level Error mode select1*	Board level Error mode select0*	0	AxisX P2 bus addr bit A3	AxisX P2 bus addr bit A2	AxisX P2 bus addr bit A1	AxisX P2 bus addr bit A0

* These bits are only in the Axis1 Output Control and Status register.

Bit	Bit Name	Description	Power Up or After Reset Value
B15 B14	Board level clock mode select1 Board level clock mode select0	The N1225A can provide the 10 MHz clock or receive an external clock. These two bits are board level setting for the clock, with clock mode 0 being the lsb. 00 Internal 10MHz clock used. P2 10 MHz clock line (P2–A9) not driven 01 N1225A gets the 10 MHz clock form backplane (P2–A9) 10 not recommended 11 N1225A 10 MHz clock drives P2 clock line (P2–A9) Note: When changing from internal to external clock, allow 10 ms for the board to acquire lock, then check the "Backplane 10 MHz Clock loss of lock" bit in the board level error status and reset register to verify the board is locked to the new 10 MHz source.	
B13 B12	Async mode select1 Async mode select0	These are board level bits that set the asynchronous modes (Choice of modes 0, 1, 2 or 3). Select0 is the lsb. Chapter 3, "Operating the Agilent N1225A" for an explanation of Asychronous modes.	00
B11 B10	AxisX P2 bus bit align1 Axis1 P2 bus bit align0	The position register in the N1225A has 37 bits and the P2 bus output has 36 bits. The P2 bus alignment bits determine which position register bits to send to the P2 bus. Align0 is the lsb. 00 P0 on P2 bus is lsb of position register (highest resolution of 0.15nm on P2 bus) 01 P0 on P2 bus is P1 of position register (lsb on P2 is 0.3nm) 10 P0 on P2 is P2 of position register (lsb on P2 is 0.6nm) 11 P0 on P2 is P3 of position register (lsb on P2 is 1.2nm)	See following table.

Bit	Bit Name	Description	Power Up or After Reset Value
B9 B8 B3 B2 B1 B0	AxisX P2 bus addr bits A5 through A0	These six bits set the P2 bus address used when reading Axis1 position off the P2 connector. Address bits A5 to A0 correspond to address lines A5 to A0 on rows A and C of the P2 connector. See Table 9 for pin numbering. For example, to put Axis1 position onto the P2 bus, set address lines A5 to A0 to match Axis1 P2 address bits A5 through A0 and bring ~Read (P2-A8) low. If P2 is being used, ensure that each axis on the P2 bus has its own unique address to avoid bus contention and possible damage.	See following table.
B7 B6 B5	Board level error mode select2 Board level error mode select1 Board level error mode select0	These bits determine the TTL logic sense and characteristics for the Error line on the P2 bus (P2-A4). Select0 is the lsb. “addressed” means the Error line for an axis is enabled when ~Read (P2-A8) is brought low and the P2 A5 through A0 addresses on P2 match the address in the axes P2 bus address bits A5 through A0. “not addressed” means the line goes low when the error occurs. 000 open collector, low true, not addressed 001 TTL, low true, addressed 010 TTL high true, addressed 011 TTL high true, addressed 100 open collector, low true, not addressed, latched* 101 TTL low true, addressed, latched<SuperScript>* 110 TTL high true, addressed, latched<SuperScript>* 111 TTL high true, addressed, latched<SuperScript>*	000

* While Output Hold is high the state of the error pin remains latched, even after the error has been cleared.

Default Power-up and Reset Values

Axis1 through Axis4 P2 bus alignment bits B10 and B11 set to 10	
Axis1	P2 bus addr bits A5–A0 set to 000001
Axis2	P2 bus addr bits A5–A0 set to 000011
Axis3	P2 bus addr bits A5–A0 set to 000010
Axis4	P2 bus addr bits A5–A0 set to 000100

Overflow Level Registers

32-bit Offsets for Overflow Level and Output Format Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$00BC	$02BC	$04BC	$06BC

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
														AxisX over-flow level bit1	AxisX over-flow level bit0

Bit	Bit name	Description	Power Up or After Reset Value
B1 B0	AxisX overflow level bits bit1 and bit0	These bits set position boundaries to define an "overflow" condition for an axis. 00: 37 valid bits. $-2^{36} \leq$ (valid range) $\leq 2^{36} - 1$ (range of ±10.6m) 01: 36 valid bits. $-2^{35} \leq$ (valid range) $\leq 2^{35} - 1$ (range of ±5.3m) 10: 35 valid bits. $-2^{34} \leq$ (valid range) $\leq 2^{34} - 1$ (range of ±2.64m) 11: 34 valid bits. $-2^{33} \leq$ (valid range) $\leq 2^{33} - 1$ (range of ±1.32m)	00

P2 Error Mask Registers

Each axis has these registers. The P2 error mask register works with the board level error status and reset register to determine which conditions will cause the P2 bus error line P2-A4 to go true, and for the respective axis, which error out line on the D row, will go true.

32-bit Offsets for P2 Error Mask Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$00A8	$02A8	$04A8	$06A8

Bit	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
Channel	4	3	2	1	4	3	2	1	4	3	2	1	4	3	2	1
Error Condition	AC too high P2 error mask bit				DC too high P2 error mask bit				Below squelch P2 error mask bit				Loss of Lock P2 error mask bit			

Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Axis	Reserved	Back-plane clock	Reference	Reference error bit	4	3	2	1	4	3	2	1	4	3	2	1
Error Condition	Reserved	LOL P2 error mask bit	LOL bit P2 Error Mask bit	Reference Error bit P2 Error Mask bit	Position or velocity comparator bit P2 error mask bit				Position overflow P2 error mask bit				Data not valid P2 error mask bit			

Please see "Board Level Error Status and Reset Register (32-Bit Offset $0028)" on page 112 for a definition of these bits.

	Bit name	Description	Power up or after reset value
B31 B30 B29 B28	Chan4 – Chan1 AC too high P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if AC light power into respective channel exceeds limit	0
B27 B26 B25 B24	Chan4 – Chan1 DC too high P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if DC light power into respective channel exceeds limit	0
B23 B22 B21 B20	Chan4 – Chan1 below squelch P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if AC light power into the channel falls below the user defined squelch set-point in the respective channel's squelch setting register	0
B19 B18 B17 B16	Chan4 – Chan1 loss of lock P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if a loss of lock occurs on the respective channel	0
B15	reserved		
B14	Backplane clock loss of lock P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if the board loses lock with the 10 MHz backplane	0
B13	Reference Lost Lock bit P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if the reference channel loses lock	0
B12	Reference Error bit P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if an error is detected on the reference channel	0
B11 B10 B9 B8	Axis4 – Axis1 position or velocity comparator bit P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if position or velocity goes outside user defined limits	0
B7 B6 B5 B4	Axis4 – Axis1 position overflow bit P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if Axis position overflow detected	0
B3 B2 B1 B0	Axis4 – Axis1 data not valid bit P2 Error Mask bit	Read/Write bits 0: No assertion of P2 Bus Error Line 1: Assert P2 Bus Error Line if position value from the respective axis is invalid	0

Position Comparator Registers

High/Low position comparator registers

These registers, such as comparator “A” and “B” allow you to detect if an axis position exceeds the value you set in the register. See “Comparator Configuration Registers" on page 127 for information on setting the test to be performed. The register values are updated when the LSW is written.

Offset

32-Bit Offset	Lower position limit (comparator “A”) 32-bit offset		High position limit (comparator “B”) 32-bit offset	
Axis1	$0074 (upper word)	$0078 (lower word)	$006C (upper word)	$0070 (lower word)
Axis2	$0274	$0278	$026C	$0270
Axis3	$0474	$0478	$046C	$0470
Axis4	$0674	$0678	$066C	$0670

Upper Long Word

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
reserved															

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
reserved											D36	D35	D34	D33	D32

Lower Long Word

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Bit Name	Description	Power Up or After Restart Value
Data bits D32 through D36 for upper position word for upper position limit	Read/Write. Units are lsbs, value is sign extended to 37 bits	0x0F
Data bits D32 through D36 for upper position word for lower position limit	Read/Write. Units are lsbs, value is sign extended to 37 bits	0x10
Data bits D0 through D31 for lower position word for upper position limit	Read/Write. Units are lsbs	0xFFFF_FFFF
Data bits D0 through D31 for lower position word for lower position limit	Read/Write. Units are lsbs, value is sign extended to 37 bits	0x0000_0000

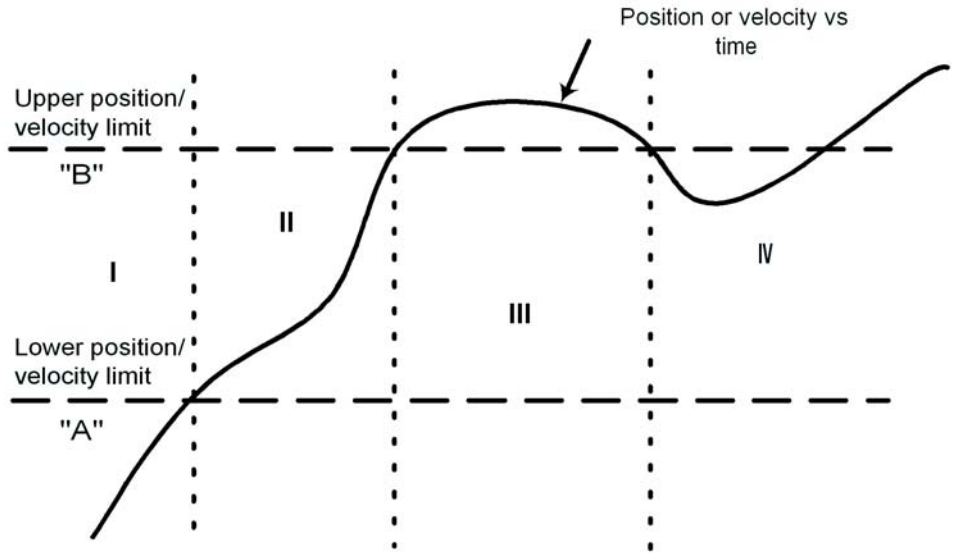


Figure 43 Comparator graph

See “Comparator Configuration Registers" on page 127 for information on programming the trigger in regions I–IV, as shown in Figure 43.

Position Preset Registers

Each axis has a position preset register. The position counter for an axis is set to this value when the position preset bit in the general control and status register is set and the axis is reset using software or hardware. The least significant bit in this register is 0.15 nm (plane mirror).

32-Bit Offset	Axis 1	Axis 2	Axis 3	Axis 4
Upper long word	$0080	$0280	$0480	$0680
Lower long word	$0084	$0284	$0484	$0684

Upper Long Word

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
reserved															

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
reserved											D36	D35	D34	D33	D32

Lower Long Word

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Bit name	Description	Power Up or After Reset Value
Data bits D32 through D36 for upper word	Read/Write. Units are lsbs,	0
Data bits D0 through D31 for lower word	Read/Write. Units are lsbs	0

Position1–Position6 Registers (Auto-Sampling)

Position1 through position6 and extended position registers

Each axis has these read-only registers, which automatically take a position sample when the most significant word (16-bit) or long word is read from the auto-sample position registers. Auto-sampling takes a position sample when the “auto sampling” position register is read, and like the regular position registers, the auto-sampled registers hold 32-bits (in twos complement form) of a 37-bit position word with the auto-sampling position extended registers holding the remaining bits (sign extended to 32-bits).

Refer to the tables below for the register address offsets.

	Axis1 offset	Axis2 offset	Axis3 offset	Axis4 offset
Position1	$0144	$0344	$0544	$0744
Position2	$014C	$034C	$054C	$074C
Position3	$0154	$0354	$0554	$0754
Position4	$015C	$035C	$055C	$075C
Position5	$0164	$0364	$0564	$0764
Position6	$016C	$036C	$056C	$076C

	Axis1 offset	Axis2 offset	Axis3 offset	Axis4 offset
ExtPosition1	$0140	$0340	$0540	$0740
ExtPosition2	$0148	$0348	$0548	$0748
ExtPosition3	$0150	$0350	$0550	$0750
ExtPosition4	$0158	$0358	$0558	$0758
ExtPosition5	$0160	$0360	$0560	$0760
ExtPosition6	$0168	$0368	$0568	$0768

NOTE

When using the Auto-Sample feature, the delay bit in the Sample Delay register for the Position or Velocity register being read should be set to one.

Position1–Position6 Registers (Standard Sampling)

Each axis has these read only registers. The position registers hold 32 bits (in twos complement form) of a 37 bit position word with the position extended registers holding the remaining bits (bits 37–32).

Refer to the tables below for the register address offsets.

Position Register 32-bit Offset Values for Position1–Position6

	Axis1 offset	Axis2 offset	Axis3 offset	Axis4 offset
Position1	$0104	$0304	$0504	$0704
Position2	$010C	$030C	$050C	$070C
Position3	$0114	$0314	$0514	$0714
Position4	$011C	$031C	$051C	$071C
Position5	$0124	$0324	$0524	$0724
Position6	$012C	$032C	$052C	$072C

Extended Position Register 32-Bit Offset Values for Position1–Position6

	Axis1 offset	Axis2 offset	Axis3 offset	Axis4 offset
ExtPosition1	$0100	$0300	$0500	$0700
ExtPosition2	$0108	$0308	$0508	$0708
ExtPosition3	$0110	$0310	$0510	$0710
ExtPosition4	$0118	$0318	$0518	$0718
ExtPosition5	$0120	$0320	$0520	$0720
ExtPosition6	$0128	$0328	$0528	$0728

Power Level Registers

Channels 1–4 AC & DC Power Level Registers

32-bit Offsets for Power Level Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$0014	$0214	$0414	$0614

AC Power Level Register

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

DC Power Level Register

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Bit name	Description	Power Up or After Reset Value
B31 through B16	Read only. Measurement of AC power into the Channel1 receiver. Range is 0 to 11468 (0 to 70 µW)	N/A
B15 through B0	Read only. Measurement of DC (total) power into the Channel1 receiver. Range is 0 to 30719 (0 to 187.5 µW)	N/A

NOTE

Power level measurements are useful as indicators only. For the best accuracy a power meter is recommended.

The power level measurement depends on the measurement algorithm being locked to the incoming light signal. If a channel has a loss of lock condition, the power level will read zero, even though a signal can be observed at the oscilloscope probe connector of the channel.

Sample Delay Register

These registers affect time delay when reading values from the 6 position and 2 velocity registers over the VMEbus, in those cases when the ~Sample1 though ~Sample4 P2 hardware inputs are used to sample position data. They do not affect data age, but instead allow the designer to know and possibly compensate for age of the position sample when it is read over the VMEbus.

In one instance, setting a “1” makes that data value available for reading over VMEbus 100ns after the ~SampleX line is brought low, and that data is stage position 2.951 µs before the ~Sample line was brought low. In the other case, setting a “0” requires waiting 2.8 µs after ~SampleX brought low, and the data read is stage position 0.251 µs before the ~SampleX line was brought low.

32-Bit Offsets for Sample Delay Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$0098	$0298	$0498	$0698

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
								Vel2	Vel1	Pos6	Pos5	Pos4	Pos3	Pos2	Pos1

Bit	Bit name	Description	Power Up or After Reset Value
B7 B6 B5 B4 B3 B2 B1 B0	Vel2 Vel1 Pos6 Pos5 Pos4 Pos3 Pos2 Pos1	Read/write 0: The data sample is available to be read over VMEbus 2.8 µs after the ~SampleX line is brought low; the data sample reported is the position value measured 251 ns before the the ~SampleX line was brought low. 1: The data is available to be read 100 ns or more after the ~SampleX line is brought low, and is the position 2.951 µs prior to ~SampleX being brought low. A graph is shown in Chapter 8, “VMEbus Data Age Timing" on page 237.	0

Sample Mode and Mask Registers

The Sample mode and mask register is a 16-bit register that combines two 8-bit registers, specifically the 8-bit “Sample Mode register” and the 8-bit “Sample Mask register”.

32-bit Offsets for Sample Mode and Mask Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$009C	$029C	$049C	$069C

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Vel2 sample mode	Vel1 sample mode	Pos6 sample mode	Pos5 sample mode	Pos4 sample mode	Pos3 sample mode	Pos2 sample mode	Pos1 sample mode	Vel2 IRQ enable	Vel1 IRQ enable	Pos6 IRQ enable	Pos5 IRQ enable	Pos4 IRQ enable	Pos3 IRQ enable	Pos2 IRQ enable	Pos1 IRQ enable

Bit	Bit name	Description	Power up or after reset value
B15 B14	AxisX Vel2 sample mode Vel2 sample mode	Read/write See Figure 24 on page 70 for more information	0
B13 B12 B11 B10 B9 B8	AxisX Pos6 sample mode Pos5 sample mode Pos4 sample mode Pos3 sample mode Pos2 sample mode Pos1 sample mode	Read/write. In any bit position: see Figure 24 on page 70 for more information	0
B7 B6	AxisX Vel2 IRQ enable Vel1 IRQ enable	Read/Write. In any bit position: 1: IRQ will be generated 0: no IRQ	0
B5 B4 B3 B2 B1 B0	AxisX Pos6 IRQ enable Pos5 IRQ enable Pos4 IRQ enable Pos3 IRQ enable Pos2 IRQ enable Pos1 IRQ enable	Read/Write. In any bit position: 1: IRQ will be generated 0: no IRQ	0

The Sample Mode register basically controls whether or not the position (1–6) and velocity (1–2) will be updated each time a sample operation is performed. See “Sampling/Reading Data over VME" on page 67 for a description of how this operates.

The Sample Mask register bits control whether a VME interrupt will be generated when a new position or velocity value is ready for reading. See “Sampling/Reading Data over VME" on page 67 for more details.

Sample Status Registers

Each axis has its own Sample status register. This read only register monitors the position (1–6) and velocity (1–2) registers sample and VME read state or status. For example, when register Position1 for Axis1 is sampled (current position has been copied into it), then bit0, the Position1 status bit becomes "1". This status bit remains "1" until the least significant word of the Axis1 Position1 register is read over the VMEbus, for D16 access, or the least significant word is read, for D32 access. Then the Axis1 Sample Status bit for Position1 is cleared.

32-bit Offsets for Sample Status Register	Axis 1	Axis 2	Axis 3	Axis 4
	$00A0	$02A0	$04A0	$06A0

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
								Vel2 status bit	Vel1 status bit	Pos6 status bit	Pos5 status bit	Pos4 status bit	Pos3 status bit	Pos2 status bit	Pos1 status bit

Bit	Bit name	Description	Power Up or After Reset Value
B7 B6	AxisX Vel2 Status bit Vel1 Status bit	Read/Write. In any bit position: 1 register has been sampled (updated with new value 0: register has been read over VMEbus, or no updating has occurred	0
B5 B4 B3 B2 B1 B0	AxisX Pos6 Status bit Pos5 Status bit Pos4 Status bit Pos3 Status bit Pos2 Status bit Pos1 Status bit	Read/Write. In any bit position 1: register has been sampled (updated with new value 0: register has been read over VMEbus, or no updating has occurred	0

Setup Registers

Axes 1–4 Setup Registers

32-bit Offsets for Axis Setup Registers	Axis 1	Axis 2	Axis 3	Axis 4
	$0024	$0224	$0424	$0624

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
NLC enable bit	0	0	AxisX D row reset enable	0			Board Level Axis D row error out config bit*			Axis P2 data bus enable bit*	All axes high speed data outputs enable*		AxisX pos bit align bit2	AxisX pos bit align bit1	AxisX pos bit align bit0

* This bit is only in the Axis1 register.

Bit	Bit name	Description	Power Up or After Reset Value
	B31 through B16	Read only bits, set to 0	0
B15	NLC enable bit	Read/write bit. (For boards with Option 200 (Non-Linearity Correction (NLC) option only)). Refer to Chapter 3, "Operating the Agilent N1225A" for a description of this option. 0: NLC disabled for this axis 1: NLC enabled for this axis	0
B12	Axis D row reset enable	Read/write bit. When set, it allows a low TTL level on the D row ~Axis reset pin for the respective axis to reset that axes position. 0: D row axis reset disabled 1: enabled	0
B8	Board Level Axis D row error output configuration bit	Read/write bit. This bit only appears in the Axis1 setup register, and sets the output mode for all axes error out pin on row D of the P2 connector. If "1", the output is "true" for any error that has been enabled using the P2 error mask register. 0: TTL low true 1: TTL high true	0
B5	Axis P2 data bus enable bit	Read/write bit. This bit only appears in the Axis1 setup register, but controls P2 data bus output for all axes. Used as an ON/OFF switch for P2 bus A and C row outputs (specifically, P35-P0, and Error line on P2 rows A and C only) 0: outputs disabled (no output regardless of P2 address bus or status of ~Read line) 1: P2 outputs can be enabled (when state of P2 address lines and ~Read line is low)	0

B4	Axis high speed data output enable	Read/Write bit. This bit only appears in the Axis1 setup register, but controls High Speed Data Outputs for all axes. 0: outputs off 1: high speed position outputs on	0
 B2 B1 B0	Axis pos bit align bits bit2 bit1 bit0	Read/Write bit. These three bits determine which 32 bits of the 37 bits in the position register are written to the 32-bit position registers, position1 through position6, for this axis. 000: This setting puts the position register lsb at the lsb of the position1 through position6 registers, making the plane mirror resolution as read from pos1 through pos6 be 0.15nm. 000: 0.15 nm resolution 001: 0.3 nm resolution 010: 0.6 nm resolution 011: 1.2 nm resolution 100: 2.4 nm resolution 101: 4.8 nm resolution 110: 4.8 nm resolution 111: 4.8 nm resolution	010

NOTE

To choose which bits are written to the P2 bus hardware outputs each axis has two sets of position bit alignment bits, one set as described here in the Setup Register and another set in the "Output Control and Status Register" on page 145.

Subnet Mask Address Register (32-Bit Offset $004C)

One 32-bit register holds the subnet mask using this format:

SNM[3].SNM[2].SNM[1].SNM[0]

16-Bit Offset	B15–B8	B7–B0
$004C	SNM[3]	SNM[2]
$004E	SNM[1]	SNM[0]

Velocity Comparator Registers

High/Low Velocity Comparator Registers

These registers allow you to detect if an axes velocity exceeds the value you set in the register. See the "Comparator Configuration Registers" on page 127 section for information on setting the test to be performed. The value in the register is updated when the LSW is written.

Axis	Low velocity limit (comparator "A") 32-bit word offset	High velocity limit (comparator "B") 32-bit word offset
Axis1	$0068	$0064
Axis2	$0268	$0264
Axis3	$0468	$0464
Axis4	$0668	$0664

B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16
reserved					D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Bit name	Description	Power up or after reset value
Data bits D0 through D26 for low velocity limit	Read/Write. Velocity data is 27 bits, twos complement (sign extended) Units: 1 lsb = lambda/(4 * 2^{24} * 100ns) = 94.3 nm/s	0x4000000
Data bits D0 through D27 for high velocity limit	Read/Write. See above for units.	0x3FFFFFF

Velocity Registers (Auto-Sampling)

Auto-sampling axes velocity1 and velocity2 registers

These registers operate the same as auto-sampling position registers.

This item is of particular concern when using 16-bit addressing and auto-sampling. The velocity value is auto-sampled when the high order 16-bits of the velocity auto-sampling register are read. To prevent a situation where the upper 16-bits read are from a current sample and the lower 16-bits are from a later sample always read the least significant 16-bits first when using 16-bit addressing.

If 32-bit reads are being performed, this timing issue will not occur.

NOTE When using the Auto-Sample feature, the delay bit in the Sample Delay register for the Position or Velocity register being read must be set to one.

Units: 1 lsb = lambda/$(4 * 2^{24} * 100\text{ns})$ = 94.3 nm/s (plane mirror)

Position Register 32-bit Offset Values for Velocity1 and Velocity2

	Axis1	Axis2	Axis3	Axis4
Velocity1	$0170	$0370	$0570	$0770
Velocity2	$0174	$0374	$0574	$0774

Velocity Registers (Standard Sampling)

Each axis has these read only registers. Velocity data is 27 bits, twos complement (sign extended).

Units: 1 lsb = lambda/(4 * 2^{24} * 100ns) = 94.3 nm/s (plane mirror)

Position Register 32-Bit Offset Values for Velocity1 and Velocity2

	Axis1	Axis2	Axis3	Axis4
Velocity1	$0130	$0330	$0530	$0730
Velocity2	$0134	$0334	$0534	$0734

Address Maps

This section provides the Agilent 1225A address maps. The summary address map is presented first (see Figure 44), and then the detailed address maps are presented.

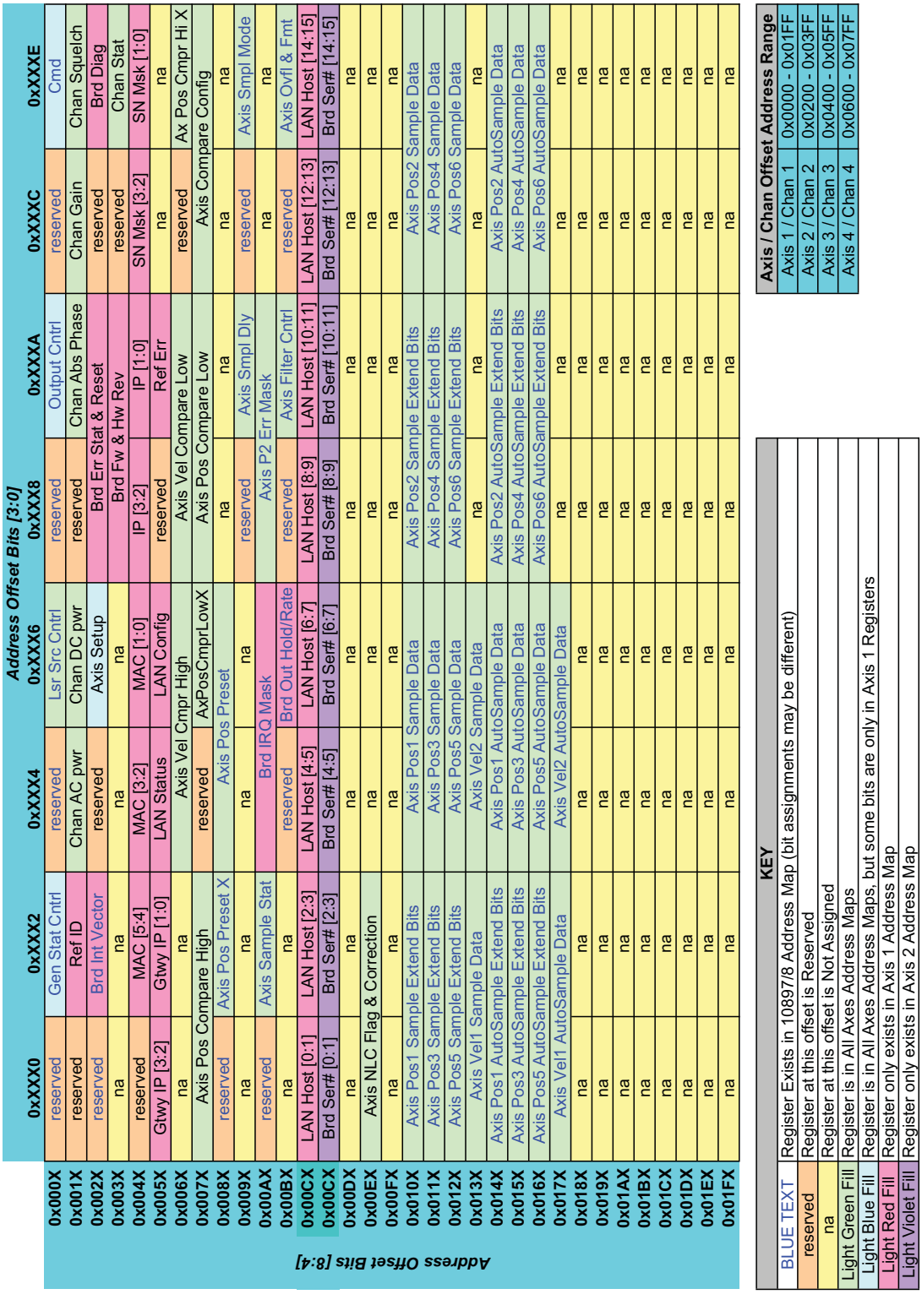


Figure 44 Single Axis Address Offset Summary for the Agilent N1225A

N1225A Address Maps

										locations used by 10898A address map			Bits, registers, addresses added to 10897/8 address map for N1225A			Non-Consistent bits or registers. These registers are not repeated at each axis location			Consistent bits or registers. These registers are repeated at each axis	
Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*	$0000	R/W or as specified	Axis1 General control and status register	partial	reserved															
2		$0002	R/W or as specified	Axis1 General control and status register	partial	x	Chan1 high temp. read only	Axis1 Signal A read only	Axis1 Signal B read only		Axis1 sample pending read only	Axis1 Position reset disable	Axis1 force 0 disable	Status LED	Axis1 Preset enable	HW Sample mode 1	HW Sample mode 0	Board level IRQ Enable	Board interrupt level bit2	Board interrupt level bit1	Board interrupt level bit 0
4	*	$0004	R/W	Axis1 Laser source control register	yes	reserved															
6		$0006	R/W	Axis1 Laser source control register	yes								Axis1 Direction Sense	Axis1 MeasA select3	Axis1 MeasA select2	Axis1 MeasA select1	Axis1 MeasA select0	Axis1 MeasB select3	Axis1 MeasB select2	Axis1 MeasB select1	Axis1 MeasB select0
8	*	$0008	R/W	Axis1 Output control and status register 0	partial	reserved															
10		$000A	R/W	Axis1 Output control and status register 0	partial	Board level clock mode select1	Board level clock mode select0	Board level async mode select1	Board level async mode select0	Axis1 P2 Bus bit alignment bit1	Axis1 P2 Bus bit alignment bit 0	Axis1 P2 Bus address bit A5	Axis1 P2 Bus address bit A4	Board level error mode select2	Board level error mode select1	Board level error mode select0	0	Axis1 P2 Bus address bit A3	Axis1 P2 Bus address bit A2	Axis1 P2 Bus address bit A1	Axis1 P2 Bus address bit A0
12	*	$000C	W	Axis1 Command Register	yes	reserved															
14		$000E	W	Axis1 Command Register	yes	x	All Axes Reset Bit	Sample Axis1 absolute phase	Drive sample4	Drive sample3	Drive sample2	Drive sample1	Reset Axis1 position	Sample Axis1 velocity2	Sample Axis1 velocity1	Sample Axis1 position6	Sample Axis1 position5	Sample Axis1 position4	Sample Axis1 position3	Sample Axis1 position2	Sample Axis1 position1
16	*	$0010	R	Reference ID register	no	reserved															
18		$0012	R	Reference ID register	no													RefID bit3	RefID bit2	RefID bit1	RefID bit 0
20	*	$0014	R	Chan1 AC power level	yes	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
22		$0016	R	Chan1 DC power level	yes	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
24	*	$0018	R	Axis1 absolute phase measurement	yes	reserved															
26		$001A	R	Axis1 absolute phase measurement	yes							B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
28	*	$001C	R/W	Chan1 gain setting	yes									reserved	reserved	reserved	Chan1 APD gain setting bit4	Chan1 APD gain setting bit3	Chan1 APD gain setting bit2	Chan1 APD gain setting bit1	Chan1 APD gain setting bit0
30		$001E	R/W	Chan1 squelch setting	yes	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
32	*	$0020	R/W	Board Level Interrupt vector register	no	reserved															
34		$0022	R/W	Board Level Interrupt vector register	no									Int vector bit7	Int vector bit6	Int vector bit5	Int vector bit4	Int vector bit3	Int vector bit2	Int vector bit1	Int vector bit0
36	*	$0024	R/W	Axis1 setup register	partial	reserved															
38		$0026	R/W	Axis1 setup register	partial	NLC Enable bit			Axis1 D row reset enable				Board level D row error out config bit			All axes P2 bus data output enable bit	All axes high speed data outputs enable		Axis1 pos bit align bit2	Axis1 pos bit align bit1	Axis1 pos bit align bit 0
40	*	$0028	R/W	Board level error status and reset register	no	Chan4 AC too high	Chan3 AC too high	Chan2 AC too high	Chan1 AC too high	Chan4 DC too high	Chan3 DC too high	Chan2 DC too high	Chan1 DC too high	Chan4 below squelch	Chan3 below squelch	Chan2 below squelch	Chan1 below squelch	Chan4 loss of lock	Chan3 loss of lock	Chan2 loss of lock	Chan1 loss of lock
42		$002A	R/W	Board level error status and reset register	no	reserved	Backplane 10MHz clock lol	Reference lost lock bit	Reference error bit	Axis4 position or velocity comparator bit	Axis3 position or velocity comparator bit	Axis2 position or velocity comparator bit	Axis1 position or velocity comparator bit	Axis4 position overflow	Axis3 position overflow	Axis2 position overflow	Axis1 position overflow	Axis4 data not valid	Axis3 data not valid	Axis2 data not valid	Axis1 data not valid
44	*	$002C	R	Board level diagnostics register	no	reserved															
46		$002E	R	Board level diagnostics register	no	reserved											+50V O.K.	-12V O.K.	+12V O.K.	reserved	+3.3V O.K.
48	*	$0030																			
56	*	$0038	R	Board Firmware/HW revision register	no	Hardware ASCII Major Version								Hardware ASCII Minor Version				Hardware ASCII Minor Version			
58		$003A	R	Board Firmware/HW revision register	no	Firmware ASCII Major Version								Firmware ASCII Minor Version				Firmware ASCII Minor Version			
60	*	$003C	R	Chan1 Status/ Diagnostics	yes																
62		$003E	R	Chan1 Status/ Diagnostics	yes			Chan1 APD temp bit13	Chan1 APD temp bit12	Chan1 APD temp bit11	Chan1 APD temp bit10	Chan1 APD temp bit9	Chan1 APD temp bit8	Chan1 APD temp bit7	Chan1 APD temp bit6	Chan1 APD temp bit5	Chan1 APD temp bit4	Chan1 APD temp bit3	Chan1 APD temp bit2	Chan1 APD temp bit1	Chan1 APD temp bit0
64	*	$0040	R	MAC address	no	reserved															
66		$0042	R	MAC address	no	MAC[5]								MAC[4]							
68	*	$0044	R	MAC address	no	MAC[3]								MAC[2]							
70		$0046	R	MAC address	no	MAC[1]								MAC[0]							
72	*	$0048	R or R/W	IP address	no	IP[3]								IP[2]							
74		$004A	R or R/W	IP address	no	IP[1]								IP[0]							

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
76	*	$004C	R or R/W	Subnet mask	no	SNM[3]								SNM[2]							
78		$004E	R or R/W	Subnet mask	no	SNM[1]								SNM[0]							
80	*	$0050	R or R/W	Gateway IP addr	no	GIP[3]								GIP[2]							
82		$0052	R or R/W	Gateway IP addr	no	GIP[1]								GIP[0]							
84	*	$0054	R	LAN status/config register (status)	no								LAN active	reserved			Static IP settings accepted	reserved	DHCP renewed	DHCP released	DHCP enabled
86		$0056	W	LAN status/config register (configuration)	no									reserved			Static IP settings accept	reserved	DHCP renew	DHCP release	DHCP enable
88	*	$0058	R	Reference error register	no																
90		$005A	R	Reference error register	no											Return clock lost status bit	Early clock lost status bit	Passed ref channel AC too high	Passed ref channel DC too high	Passed ref channel below squelch	Passed ref channel loss of lock
92	*	$005C																			
100	*	$0064	R/W	Axis1 velocity comparator high	yes	reserved					D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
102		$0066	R/W	Axis1 velocity comparator high	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
104	*	$0068	R/W	Axis1 velocity comparator low	yes	reserved					D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
106		$006A	R/W	Axis1 velocity comparator low	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
108	*	$006C	R/W	Axis1 position comparator high	yes	reserved															
110		$006E	R/W	Axis1 position comparator high	yes	reserved											D36	D35	D34	D33	D32
112	*	$0070	R/W	Axis1 position comparator high	yes	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
114		$0072	R/W	Axis1 position comparator high	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
116	*	$0074	R/W	Axis1 position comparator low	yes	reserved															
118		$0076	R/W	Axis1 position comparator low	yes	reserved											D36	D35	D34	D33	D32
120	*	$0078	R/W	Axis1 position comparator low	yes	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
122		$007A	R/W	Axis1 position comparator low	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
124	*	$007C	R/W	Axis1 comparator config	yes			Axis1 bd level err reg comp output bit select bit1	Axis1 bd level err reg comp output bit select bit0	Axis1 velocity comp latched result	Axis1 velocity comp realtime result	Axis1 velocity comp result config bit1	Axis1 velocity comp result config bit0		Axis1 velocity comp B test bit2	Axis1 velocity comp B test bit1	Axis1 velocity comp B test bit0		Axis1 velocity comp A test bit2	Axis1 velocity comp A test bit1	Axis1 Velocity Comp A test bit0
126		$007E	R/W	Axis1 comparator config	yes	All Axes D row comparator and error output enable	Axis1 D row comparator out config bit2	Axis1 D row comparator out config bit1	Axis1 D row comparator out config bit0	Axis1 position comp latched result	Axis1 position comp realtime result	Axis1 position comp result config bit1	Axis1 position comp result config bit0		Axis1 position comp B test bit2	Axis1 position comp B test bit1	Axis1 position comp B test bit0		Axis1 position comp A test bit2	Axis1 position comp A test bit1	Axis1 position Comp A test bit0
128	*	$0080	R/W	Axis1 position preset MSB's register	yes	reserved															
130		$0082	R/W	Axis1 position preset MSB's register	yes	reserved											D36	D35	D34	D33	D32
132	*	$0084	R/W	Axis1 position preset LSB's register (D31-D16)	yes	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
134		$0086	R/W	Axis1 position preset LSB's register (D15-D00)	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
136	*	$0088																			
152	*	$0098	R/W	Axis1 Sample delay register	yes	reserved															
154		$009A	R/W	Axis1 Sample delay register	yes									velocity2	velocity1	position6	position5	position4	position3	position2	position1
156	*	$009C	R/W	Axis1 Sample mode and mask register	yes	reserved															
158		$009E	R/W	Axis1 Sample mode and mask register	yes	velocity2 sample mode	velocity1 sample mode	position6 sample mode	position5 sample mode	position4 sample mode	position3 sample mode	position2 sample mode	position1 sample mode	velocity2 IRQ enable	velocity1 IRQ enable	position6 IRQ enable	position5 IRQ enable	position4 IRQ enable	position3 IRQ enable	position2 IRQ enable	position1 IRQ enable
160	*	$00A0	R	Axis1 Sample status register	yes	reserved															
162		$00A2	R	Axis1 Sample status register	yes	x	x	x	x	x	x	x	x	Axis1 velocity2 status bit	Axis1 velocity1 status bit	Axis1 position6 status bit	Axis1 position5 status bit	Axis1 position4 status bit	Axis1 position3 status bit	Axis1 position2 status bit	Axis1 position1 status bit
164	*	$00A4	R/W	Board level IRQ Error mask register	no	Chan4 AC too high IRQ error mask bit	Chan3 AC too high IRQ error mask bit	Chan2 AC too high IRQ error mask bit	Chan1 AC too high IRQ error mask bit	Chan4 DC too high IRQ error mask bit	Chan3 DC too high IRQ error mask bit	Chan2 DC too high IRQ error mask bit	Chan1 DC too high IRQ error mask bit	Chan4 below squelch IRQ error mask bit	Chan3 below squelch IRQ error mask bit	Chan2 below squelch IRQ error mask bit	Chan1 below squelch IRQ error mask bit	Chan4 loss of lock IRQ error mask bit	Chan3 loss of lock IRQ error mask bit	Chan2 loss of lock IRQ error mask bit	Chan1 loss of lock IRQ error mask bit
166		$00A6	R/W	Board level IRQ Error mask register	no	reserved	Backplane 10MHz clock lol IRQ error mask bit	Reference lost lock bit IRQ error mask bit	Reference error bit IRQ error mask bit	Axis4 position or velocity comparator bit IRQ error mask bit	Axis3 position or velocity comparator bit IRQ error mask bit	Axis2 position or velocity comparator bit IRQ error mask bit	Axis1 position or velocity comparator bit IRQ error mask bit	Axis4 position overflow IRQ error mask bit	Axis3 position overflow IRQ error mask bit	Axis2 position overflow IRQ error mask bit	Axis1 position overflow IRQ error mask bit	Axis4 data not valid IRQ error mask bit	Axis3 data not valid IRQ error mask bit	Axis2 data not valid IRQ error mask bit	Axis1 data not valid IRQ error mask bit

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
168	*	$00A8	R/W	Axis1 P2 Error mask register	yes	Chan4 AC too high P2 error mask bit	Chan3 AC too high P2 error mask bit	Chan2 AC too high P2 error mask bit	Chan1 AC too high P2 error mask bit	Chan4 DC too high P2 error mask bit	Chan3 DC too high P2 error mask bit	Chan2 DC too high P2 error mask bit	Chan1 DC too high P2 error mask bit	Chan4 below squelch P2 error mask bit	Chan3 below squelch P2 error mask bit	Chan2 below squelch P2 error mask bit	Chan1 below squelch P2 error mask bit	Chan4 loss of lock P2 error mask bit	Chan3 loss of lock P2 error mask bit	Chan2 loss of lock P2 error mask bit	Chan1 loss of lock P2 error mask bit
170		$00AA	R/W	Axis1 P2 Error mask register	yes	reserved	Backplane 10MHz clock lol P2 error mask bit	Reference lost lock bit P2 error mask bit	Reference error bit P2 error mask bit	Axis4 position or velocity comparator bit P2 error mask bit	Axis3 position or velocity comparator bit P2 error mask bit	Axis2 position or velocity comparator bit P2 error mask bit	Axis1 position or velocity comparator bit P2 error mask bit	Axis4 position overflow P2 error mask bit	Axis3 position overflow P2 error mask bit	Axis2 position overflow P2 error mask bit	Axis1 position overflow P2 error mask bit	Axis4 data not valid P2 error mask bit	Axis3 data not valid P2 error mask bit	Axis2 data not valid P2 error mask bit	Axis1 data not valid P2 error mask bit
172	*	$00AC																			
180	*	$00B4	R/W	Board level output hold and rate control register	no	reserved															
182		$00B6	R/W	Board level output hold and rate control register	no	x	x	x	x	x	x	x	x	Output hold line control	x	Async mode 2 divisor bit5	Async mode 2 divisor bit4	Async mode 2 divisor bit3	Async mode 2 divisor bit2	Async mode 2 divisor bit1	Async mode 2 divisor bit0
184	*	$00B8	R/W	Axis1 Filter control register	yes	reserved															
186		$00BA	R/W	Axis1 Filter control register	yes	reserved												K_{p1}	K_{p0}	K_{v1}	K_{v0}
188	*	$00BC	R/W	Axis1 Overflow level and output format register	yes	reserved															
190		$00BE	R/W	Axis1 Overflow level and output format register	yes	x	x	x	x	x	x	x	x	x	x	x	x	x		Axis1 overflow level1	Axis1 overflow level 0
192	*	$00C0	R/W	LAN Hostname	no	HOST[0]								HOST[1]							
194		$00C2	R/W	LAN Hostname	no	HOST[2]								HOST[3]							
196	*	$00C4	R/W	LAN Hostname	no	HOST[4]								HOST[5]							
198		$00C6	R/W	LAN Hostname	no	HOST[6]								HOST[7]							
200	*	$00C8	R/W	LAN Hostname	no	HOST[8]								HOST[9]							
202		$00CA	R/W	LAN Hostname	no	HOST[10]								HOST[11]							
204	*	$00CC	R/W	LAN Hostname	no	HOST[12]								HOST[13]							
206		$00CE	R/W	LAN Hostname	no	HOST[14]								HOST[15]							
208	*	$00D0																			
224	*	$00E0	R	Axis1 NLC Flag & phase/magnitude correction register	yes	NLC Qualified	0	0	0	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
226		$00E2	R	Axis1 NLC Flag & phase/magnitude correction register	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
228	*	$00E4																			
256	*	$0100	R	Axis1 Pos1 extended register	yes	sign extended (EXAMPLE FOR EXTENDED REGISTERS)															
258		$0102	R	Axis1 Pos1 extended register	yes	sign extended											D36	D35	D34	D33	D32
260	*	$0104	R	Axis1 Pos1 register	yes																
264	*	$0108	R	Axis1 Pos2 extended register	yes																
268	*	$010C	R	Axis1 Pos2 register	yes																

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
272	*	$0110	R	Axis1 Pos3 extended register	yes																
276	*	$0114	R	Axis1 Pos3 register	yes																
280	*	$0118	R	Axis1 Pos4 extended register	yes																
284	*	$011C	R	Axis1 Pos4 register	yes																
288	*	$0120	R	Axis1 Pos5 extended register	yes																
292	*	$0124	R	Axis1 Pos5 register	yes																
296	*	$0128	R	Axis1 Pos6 extended register	yes																
300	*	$012C	R	Axis1 Pos6 register	yes																
304	*	$0130	R	Axis1 Vel1 register	yes	sign extended					27 bits, sign extended										
308	*	$0134	R	Axis1 Vel2 register	yes	sign extended					27 bits, sign extended										
312	*	$0138																			
320	*	$0140	R	Axis1 Pos1 extended auto sampling	yes																
324	*	$0144	R	Axis1 Pos1 auto sampling	yes																
328	*	$0148	R	Axis1 Pos2 extended auto sampling	yes																
332	*	$014C	R	Axis1 Pos2 auto sampling	yes																
336	*	$0150	R	Axis1 Pos3 extended auto sampling	yes																
340	*	$0154	R	Axis1 Pos3 auto sampling	yes																
344	*	$0158	R	Axis1 Pos4 extended auto sampling	yes																
348	*	$015C	R	Axis1 Pos4 auto sampling	yes																
352	*	$0160	R	Axis1 Pos5 extended auto sampling	yes																
356	*	$0164	R	Axis1 Pos5 auto sampling	yes																
360	*	$0168	R	Axis1 Pos6 extended auto sampling	yes																
364	*	$016C	R	Axis1 Pos6 auto sampling	yes																
368	*	$0170	R	Axis1 Vel1 auto sampling	yes																
372	*	$0174	R	Axis1 Vel2 auto sampling	yes																
508	*	$01FC																			

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
512 1024 1536	*	$0200 $0400 $0600	R/W or as specified	AxisX General control and status register	partial	reserved															
514 1026 1538		$0202 $0402 $0602	R/W or as specified	AxisX General control and status register	partial	x	ChanX high temp. read only	AxisX Signal A read only	AxisX Signal B read only		AxisX sample pending read only	AxisX Position reset disable	AxisX Force 0 disable		AxisX Preset enable						
516 1028 1540	*	$0204 $0404 $0604	R/W	AxisX Laser source control register	yes	reserved															
518 1030 1542		$0206 $0406 $0606	R/W	AxisX Laser source control register	yes								AxisX Direction Sense	AxisX MeasA select3	AxisX MeasA select2	AxisX MeasA select1	AxisX MeasA select0	AxisX MeasB select3	AxisX MeasB select2	AxisX MeasB select1	AxisX MeasB select0
520 1032 1544	*	$0208 $0408 $0608	R/W	AxisX Output control and status register 0	partial	reserved															
522 1034 1546		$020A $040A $060A	R/W	AxisX Output control and status register 0	partial					AxisX P2 Bus bit alignment bit1	AxisX P2 Bus bit alignment bit 0	AxisX P2 Bus address bit A5	AxisX P2 Bus address bit A4				0	AxisX P2 Bus address bit A3	AxisX P2 Bus address bit A2	AxisX P2 Bus address bit A1	AxisX P2 Bus address bit A0
524 1036 1548	*	$020C $040C $060C	W	AxisX Command Register	yes	reserved															
526 1038 1550		$020E $040E $060E	W	AxisX Command Register	yes	x	x	Sample AxisX absolute phase					Reset AxisX position	Sample AxisX velocity2	Sample AxisX velocity1	Sample AxisX position6	Sample AxisX position5	Sample AxisX position4	Sample AxisX position3	Sample AxisX position2	Sample AxisX position1
528	*	$0210																			
532 1044 1556	*	$0214 $0414 $0614	R	ChanX AC power level	yes	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
534 1046 1558		$0216 $0416 $0616	R	ChanX DC power level	yes	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
536 1048 1560	*	$0218 $0418 $0618	R	AxisX absolute phase measurement	yes	reserved															
538 1050 1562		$021A $041A $061A	R	AxisX absolute phase measurement	yes							B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
540 1052 1564	*	$021C $041C $061C	R/W	ChanX gain setting	yes									reserved	reserved	reserved	ChanX APD gain setting bit4	ChanX APD gain setting bit3	ChanX APD gain setting bit2	ChanX APD gain setting bit1	ChanX APD gain setting bit0
542 1054 1566		$021E $041E $061E	R/W	ChanX squelch setting	yes	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
544	*	$0220																			
548 1060 1572	*	$0224 $0424 $0624	R/W	AxisX setup register	yes	reserved															
550 1062 1574		$0226 $0426 $0626	R/W	AxisX setup register	yes	NLC Enable bit			AxisX D row reset enable										AxisX pos bit align bit2	AxisX pos bit align bit1	AxisX pos bit align bit 0

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
568	*	$0238																			
572 1084 1596	*	$023C $043C $063C	R	ChanX Status/ Diagnostics	yes	reserved															
574 1086 1598		$023E $043E $063E	R	ChanX Status/ Diagnostics	yes	reserved		ChanX APD temp bit13	ChanX APD temp bit12	ChanX APD temp bit11	ChanX APD temp bit10	ChanX APD temp bit9	ChanX APD temp bit8	ChanX APD temp bit7	ChanX APD temp bit6	ChanX APD temp bit5	ChanX APD temp bit4	ChanX APD temp bit3	ChanX APD temp bit2	ChanX APD temp bit1	ChanX APD temp bit0
608	*	$0260																			
612 1124 1636	*	$0264 $0464 $0664	R/W	AxisX velocity comparator high	yes	reserved					D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
614 1126 1638		$0266 $0466 $0666	R/W	AxisX velocity comparator high	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
616 1128 1640	*	$0268 $0468 $0668	R/W	AxisX velocity comparator low	yes	reserved					D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
618 1130 1642		$026A $046A $066A	R/W	AxisX velocity comparator low	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
620 1132 1644	*	$026C $046C $066C	R/W	AxisX position comparator high	yes	reserved															
622 1134 1646		$026E $046E $066E	R/W	AxisX position comparator high	yes	reserved											D36	D35	D34	D33	D32
624 1136 1648	*	$0270 $0470 $0670	R/W	AxisX position comparator high	yes	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
626 1138 1650		$0272 $0472 $0672	R/W	AxisX position comparator high	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
628 1140 1652	*	$0274 $0474 $0674	R/W	AxisX position comparator low	yes	reserved															
630 1142 1654		$0276 $0476 $0676	R/W	AxisX position comparator low	yes	reserved											D36	D35	D34	D33	D32
632 1144 1656	*	$0278 $0478 $0678	R/W	AxisX position comparator low	yes	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
634 1146 1658		$027A $047A $067A	R/W	AxisX position comparator low	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
636 1148 1660	*	$027C $047C $067C	R/W	AxisX comparator config	yes			AxisX bd level err reg comp output bit select bit1	AxisX bd level err reg comp output bit select bit0	AxisX velocity comp latched result	AxisX velocity comp realtime result	AxisX velocity comp result config bit1	AxisX velocity comp result config bit0		AxisX velocity comp B test bit2	AxisX velocity comp B test bit1	AxisX velocity comp B test bit0		AxisX velocity comp A test bit2	AxisX velocity comp A test bit1	AxisX Velocity Comp A test bit0
638 1150 1662		$027E $047E $067E	R/W	AxisX comparator config	yes		AxisX D row comparator out config bit2	AxisX D row comparator out config bit1	AxisX D row comparator out config bit0	AxisX position comp latched result	AxisX position comp realtime result	AxisX position comp result config bit1	AxisX position comp result config bit0		AxisX position comp B test bit2	AxisX position comp B test bit1	AxisX position comp B test bit0		AxisX position comp A test bit2	AxisX position comp A test bit1	AxisX position Comp A test bit0

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
640 1152 1664	*	$0280 $0480 $0680	R/W	AxisX position preset MSB's register	yes	reserved															
642 1154 1666		$0282 $0482 $0682	R/W	AxisX position preset MSB's register	yes	reserved											D36	D35	D34	D33	D32
644 1156 1668	*	$0284 $0484 $0684	R/W	AxisX position preset LSB's register (D31-D16)	yes	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
646 1158 1670		$0286 $0486 $0686	R/W	AxisX position preset LSB's register (D15-D00)	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
648	*	$0288																			
652 1164 1676	*	$028C $048C $068C		Former location of clip mask		Not used															
654 1166 1678		$028E $048E $068E		Former location of clip mask		Not used															
656	*	$0290																			
664 1176 1688	*	$0298 $0498 $0698	R/W	AxisX Sample delay register	yes	reserved															
666 1178 1690		$029A $049A $069A	R/W	AxisX Sample delay register	yes									velocity2	velocity1	position6	position5	position4	position3	position2	position1
668 1180 1692	*	$029C $049C $069C	R/W	AxisX Sample mode and mask register	yes	reserved															
670 1182 1694		$029E $049E $069E	R/W	AxisX Sample mode and mask register	yes	velocity2 sample mode	velocity1 sample mode	position6 sample mode	position5 sample mode	position4 sample mode	position3 sample mode	position2 sample mode	position1 sample mode	velocity2 IRQ enable	velocity1 IRQ enable	position6 IRQ enable	position5 IRQ enable	position4 IRQ enable	position3 IRQ enable	position2 IRQ enable	position1 IRQ enable
672 1184 1696	*	$02A0 $04A0 $06A0	R	AxisX Sample status register	yes	reserved															
674 1186 1698		$02A2 $04A2 $06A2	R	AxisX Sample status register	yes	x	x	x	x	x	x	x	x	AxisX velocity2 status bit	AxisX velocity1 status bit	AxisX position6 status bit	AxisX position5 status bit	AxisX position4 status bit	AxisX position3 status bit	AxisX position2 status bit	AxisX position1 status bit
676	*	$02A4																			
680 1192 1704	*	$02A8 $04A8 $06A8	R/W	AxisX P2 Error mask register	yes	Chan4 AC too high P2 error mask bit	Chan3 AC too high P2 error mask bit	Chan2 AC too high P2 error mask bit	Chan1 AC too high P2 error mask bit	Chan4 DC too high P2 error mask bit	Chan3 DC too high P2 error mask bit	Chan2 DC too high P2 error mask bit	Chan1 DC too high P2 error mask bit	Chan4 below squelch P2 error mask bit	Chan3 below squelch P2 error mask bit	Chan2 below squelch P2 error mask bit	Chan1 below squelch P2 error mask bit	Chan4 loss of lock P2 error mask bit	Chan3 loss of lock P2 error mask bit	Chan2 loss of lock P2 error mask bit	Chan1 loss of lock P2 error mask bit
682 1194 1706		$02AA $04AA $06AA	R/W	AxisX P2 Error mask register	yes	reserved	Backplane 10MHz clock lol P2 error mask bit	Reference lost lock bit P2 error mask bit	Reference error bit P2 error mask bit	Axis4 position or velocity comparator bit P2 error mask bit	Axis3 position or velocity comparator bit P2 error mask bit	Axis2 position or velocity comparator bit P2 error mask bit	Axis1 position or velocity comparator bit P2 error mask bit	Axis4 position overflow P2 error mask bit	Axis3 position overflow P2 error mask bit	Axis2 position overflow P2 error mask bit	Axis1 position overflow P2 error mask bit	Axis4 data not valid P2 error mask bit	Axis3 data not valid P2 error mask bit	Axis2 data not valid P2 error mask bit	Axis1 data not valid P2 error mask bit

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
692	*	$02B4																			
696 1208 1720	*	$02B8 $04B8 $06B8	R/W	AxisX Filter control register	yes	reserved															
698 1210 1722		$02BA $04BA $06BA	R/W	AxisX Filter control register	yes	reserved												K_{p1}	K_{p0}	K_{v1}	K_{v0}
700 1212 1724	*	$02BC $04BC $06BC	R/W	AxisX Overflow level and output format register	yes	reserved															
702 1214 1726		$02BE $04BE $06BE	R/W	AxisX Overflow level and output format register	yes	x	x	x	x	x	x	x	x	x	x	x	x	x		AxisX overflow level1	AxisX overflow level 0
704	*	$02C0	R	Board Serial Number	no	ASCII CHAR[0]								ASCII CHAR[1]							
706		$02C2	R	Board Serial Number	no	ASCII CHAR[2]								ASCII CHAR[3]							
708	*	$02C4	R	Board Serial Number	no	ASCII CHAR[4]								ASCII CHAR[5]							
710		$02C6	R	Board Serial Number	no	ASCII CHAR[6]								ASCII CHAR[7]							
712	*	$02C8	R	Board Serial Number	no	ASCII CHAR[8]								ASCII CHAR[9]							
714		$02CA	R	Board Serial Number	no	ASCII CHAR[10]								ASCII CHAR[11]							
716	*	$02CC	R	Board Serial Number	no	ASCII CHAR[12]								ASCII CHAR[13]							
718		$02CE	R	Board Serial Number	no	ASCII CHAR[14]								ASCII CHAR[15] = 0x0 (null)							
732	*	$02DC																			
736 1248 1760	*	$02E0 $04E0 $06E0	R	AxisX NLC Flag & phase/magnitude correction register	yes	NLC Qualified	0	0	0	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
738 1250 1762		$02E2 $04E2 $06E2	R	AxisX NLC Flag & phase/magnitude correction register	yes	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
764	*	$02FC																			
768 1280 1792	*	$0300 $0500 $0700	R	AxisX Pos1 extended register	yes	sign extended (EXAMPLE FOR EXTENDED REGISTERS)															
770 1282 1794		$0302 $0502 $0702	R	AxisX Pos1 extended register	yes	sign extended											D36	D35	D34	D33	D32
772 1284 1796	*	$0304 $0504 $0704	R	AxisX Pos1 register	yes																
776 1288 1800	*	$0308 $0508 $0708	R	AxisX Pos2 extended register	yes																
780 1292 1804	*	$030C $050C $070C	R	AxisX Pos2 register	yes																
784 1296 1808	*	$0310 $0510 $0710	R	AxisX Pos3 extended register	yes																
788 1300 1812	*	$0314 $0514 $0714	R	AxisX Pos3 register	yes																

Offset (decimal)	32 bit	Offset (Hex)	R/W ?	Description	Consistency (same as other axes)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
792 1304 1816	*	$0318 $0518 $0718	R	AxisX Pos4 extended register	yes																
796 1308 1820	*	$031C $051C $071C	R	AxisX Pos4 register	yes																
800 1312 1824	*	$0320 $0520 $0720	R	AxisX Pos5 extended register	yes																
804 1316 1828	*	$0324 $0524 $0724	R	AxisX Pos5 register	yes																
808 1320 1832	*	$0328 $0528 $0728	R	AxisX Pos6 extended register	yes																
812 1324 1836	*	$032C $052C $072C	R	AxisX Pos6 register	yes																
816 1328 1840	*	$0330 $0530 $0730	R	AxisX Vel1 register	yes	sign extended					27 bits, sign extended										
820 1332 1844	*	$0334 $0534 $0734	R	AxisX Vel2 register	yes	sign extended					27 bits, sign extended										
828	*	$033C																			
832 1344 1856	*	$0340 $0540 $0740	R	AxisX Pos1 extended auto sampling	yes																
836 1348 1860	*	$0344 $0544 $0744	R	AxisX Pos1 auto sampling	yes																
840 1352 1864	*	$0348 $0548 $0748	R	AxisX Pos2 extended auto sampling	yes																
844 1356 1868	*	$034C $054C $074C	R	AxisX Pos2 auto sampling	yes																
848 1360 1872	*	$0350 $0550 $0750	R	AxisX Pos3 extended auto sampling	yes																
852 1364 1876	*	$0354 $0554 $0754	R	AxisX Pos3 auto sampling	yes																
856 1368 1880	*	$0358 $0558 $0758	R	AxisX Pos4 extended auto sampling	yes																
860 1372 1884	*	$035C $055C $075C	R	AxisX Pos4 auto sampling	yes																
864 1376 1888	*	$0360 $0560 $0760	R	AxisX Pos5 extended auto sampling	yes																
868 1380 1892	*	$0364 $0564 $0764	R	AxisX Pos5 auto sampling	yes																

5 Hardware Interface

Introduction

This chapter provides signal information needed to connect the N1225A to a customer provided or designed board. It provides pin-outs for N1225A connectors, recommended terminations for signal lines, and format for data words. Also included is information on how various register settings and board conditions are related to the hardware outputs.

Front and Back Connectors

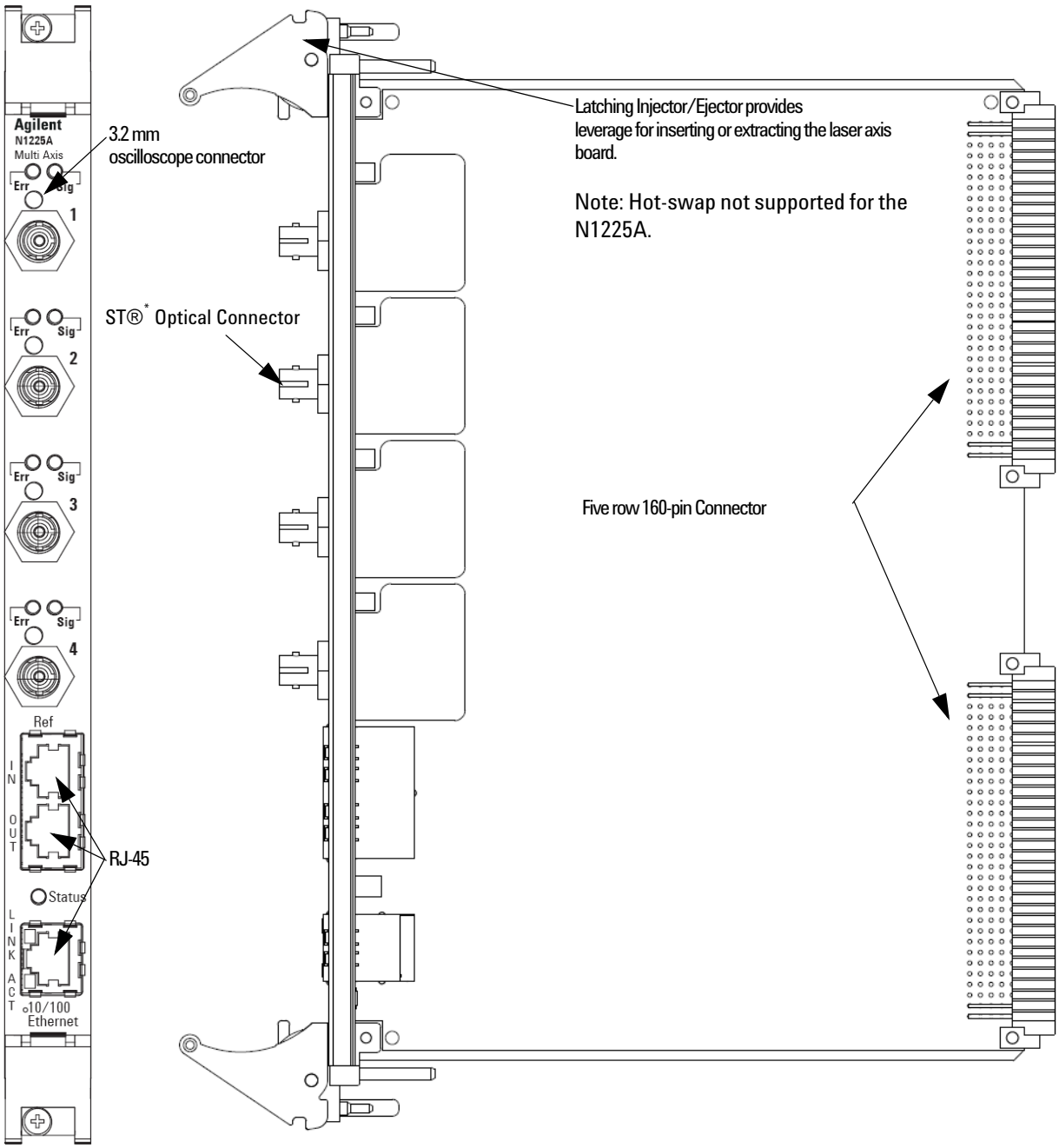


Figure 45 N1225A front and back view

Front Connector Pin-Out

3.2 mm oscilloscope probe socket

The center socket is connected to the output of the first stage photodiode amplifier output through a 100Ω resistor.

The shell is connected to analog ground.

Reference In and Reference Out connectors (RJ-45)

Pins	Wiring
1–2	Clock in
5–4	Clock out (80 MHz)
3–6	Data 0 (80 MHz maximum) in/out
7–8	Data 1 (80 MHz maximum) in/out

Signals are LVPECL. this information is provided for reference only.

CAUTION The reference in/out connector should be connected only to another N1225A or compatible product.

10/100 BaseT Ethernet connector (RJ-45)

Pins	Wiring
4–5	Pair 1
1–2	Pair 2
3–6	Pair 3
7–8	Pair 4

Back Connector Pin-Out (P1)

This is the standard VMEbus pinout.

CAUTION Not all pins are used. Unused pins are either held in a high impedance state or are not connected. Do not apply voltages outside the TTL range to these pins.

P1 Bus Pinout

pin #	Row Z	Row A	Row B	Row C	Row D
Where: BG0IN* tied to BG0OUT*;BG01N* tied to BG1OUT*;BG2IN* tied to BG2OUT*;BG3IN* tied to BG3OUT*					
1	—[1]	D00	—[1]	D08	—[1,2]
2	GND	D01	—[1]	D09	GND[2]
3	—[1]	D02	—[1]	D10	—
4	GND	D03	~BG0IN	D11	—
5	—[1]	D04	~BG0OUT	D12	—
6	GND	D05	~BG1IN	D13	—
7	—[1]	D06	~BG1OUT	D14	—
8	GND	D07	~BG2IN	D15	—
9	—[1]	GND	~BG2OUT	GND	~GAP
10	GND	—[1]	~BG3IN	—[1]	~GA0
11	—[1]	GND	~BG3OUT	~BERR	~GA1
12	GND	~DS1	—[1]	~SYSRESET[3]	—[1]
13	—[1]	~DS0	—[1]	~LWORD	~GA2
14	GND	~WRITE	—[1]	AM5	—[1]
15	—[1]	GND	—[1]	A23	~GA3
16	GND	~DTACK	AM0	A22	—[1]
17	—[1]	GND	AM1	A21	~GA4
18	GND	~AS	AM2	A20	—[1]
19	—[1]	GND	AM3	A19	—[1]
20	GND	~IACK	GND	A18	—[1]
21	—[1]	~IACKIN	—[1]	A17	—[1]
22	GND	~IACKOUT	—[1]	A16	—[1]
23	—[1]	AM4	GND	A15	—[1]
24	GND	A07	~IRQ7	A14	—[1]
25	—[1]	A06	~IRQ6	A13	—[1]
26	GND	A05	~IRQ5	A12	
27	—[1]	A04	~IRQ4	A11	—[1]
28	GND	A03	~IRQ3	A10	—[1]
29	—[1]	A02	~IRQ2	A09	—[1]
30	GND	A01	~IRQ1	A08	—[1]
31	—[1]	—[1]	—[1]	—[1]	GND
32	GND	+5V	+5V	+5V	—[1,2]

[1] Blank means not connected or high impedance state. Do not apply voltage outside the TTL range to these pins.
[2] Pins are MFBL.
[3] Pulling ~SYSRESET low initiates a hard reboot of the board.

P2 Bus Pin-Out Information for User-Defined Pins

This section includes information for:

- Rows A and C of P2, since these rows are compatible with the 10898A and partially compatible with the 10897A/B/C boards.
- Rows Z and D which are used for additional functions.

P2 Bus Pinout

Table 9 P2 Bus Pinout

pin #	Row Z	Row A	Row B	Row C	Row D
1	Axis2_P0	A4	+5V	GND	Axis3_P6[1]
2	GND	A5	GND	GND	Axis3_P7[1]
3	Axis2_P1	AOH/OCLK	RESERVED	GND	Axis3_P8
4	GND	Error	—[2]	~Sample1	Axis3_P9
5	Axis2_P2	—[2]	—[2]	~Sample2	Axis4_P0
6	GND	~Force Zero	—[2]	~Sample3	Axis4_P1
7	Axis2_P3	~Position Reset	—[2]	~Sample4	Axis4_P2
8	GND	~Read	—[2]	Output Hold	Axis4_P3
9	Axis2_P4	10 MHz clock	—[2]	GND	Axis4_P4
10	GND	AxisX_P0[3]	—[2]	GND	Axis4_P5
11	Axis2_P5	AxisX_P2[3]	—[2]	AxisX_P1[3]	Axis4_P6
12	GND	AxisX_P4[3]	GND	AxisX_P3[3]	Axis4_P7
13	Axis2_P6	AxisX_P6[3]	+5V	AxisX_P5[3]	Axis4_P8
14	GND	GND	D16	AxisX_P7[3]	Axis4_P9
15	Axis2_P7	AxisX_P9[3]	D17	AxisX_P8[3]	—[2]
16	GND	AxisX_P11[3]	D18	AxisX_P10[3]	—[2]
17	Axis2_P8	AxisX_P13[3]	D19	AxisX_P12[3]	Axis1 err out
18	GND	AxisX_P15[3]	D20	AxisX_P14[3]	Axis2 err out
19	Axis2_P9	AxisX_P16[3]	D21	GND	Axis3 err out
20	GND	AxisX_P18[3]	D22	AxisX_P17[3]	Axis4 err out
21	Axis3_P0	AxisX_P20[3]	D23	AxisX_P19[3]	Axis1 Comp out
22	GND	AxisX_P22[3]	GND	AxisX_P21[3]	Axis2 Comp out
23	Axis3_P1	GND	D24	AxisX_P23[3]	Axis3 Comp out
24	GND	AxisX_P25[3]	D25	AxisX_P24[3]	Axis4 Comp out
25	Axis3_P2	AxisX_P27[3]	D26	AxisX_P26[3]	—[2]
26	GND	AxisX_P29[3]	D27	AxisX_P28[3]	—[2]
27	Axis3_P3	AxisX_P31[3]	D28	AxisX_P30[3]	~Axis1 reset in
28	GND	AxisX_P32[3]	D29	GND	~Axis2 reset in
29	Axis3_P4	AxisX_P34[3]	D30	AxisX_P33[3]	~Axis3 reset in
30	GND	A0	D31	AxisX_P35[3]	~Axis4 reset in
31	Axis3_P5	A2	GND	A1	GND[1]
32	GND	GND	+5V	A3	+5V[1]

[1] Pins are MFBL. VPC not supported, “hot swap capability” not supported.
[2] Blank means not connected or high impedance state. Do not apply voltage outside the TTL range to these pins.
[3] “AxisX”: P2 bus address, or use of high speed outputs, determines which axis’data appears on P2.

NOTE

The following pins, connected to the 74LVTH125 parts, when used as inputs must be driven or have pull-up resistors to ensure a minimum current to the pin of 0.5 mA: Force Zero Input, ~Sample1-4, ~Position Reset, Output Hold, ~Read Input, AOH/CLK I/O. Use a 6.6 kΩ (maximum) pull-up resistor. If this is not done the input logic state is unknown.

All inputs on P2 row D must have pull-up resistors, 6.6 kΩ (maximum), or be driven. This applies to the ~Axis1_reset in to ~Axis4_reset in.

NOTE

The D and Z row outputs are not addressed and should not be bussed together.

Overview for P2 rows A and C

Overview

The P2 rows A and C have been set aside by the VMEbus specification to be defined by the user. Most of the pins on the P2 outer rows are associated with the Hardware Position output and its data transfer, communication and control interface to user hardware. The exceptions are the 10 MHz Clock pin which provides or accepts the system clock and the ~Sample1 to ~Sample4 pins which allow hardware sampling of position data that is to be transferred over VMEbus. These pins are also described here.

All backplane I/O signals are TTL-compatible. Signal and bus timing and pin currents are provided in the specifications.

10 MHz Clock Input/Output Pin

This pin provides either the system clock to other N1225A boards, or is programmed to accept a system clock from an external source. It is programmed either as input or as an output via the Output Control register. When programmed as an output, the N1225A board drives the 10 MHz Clock pin from its local crystal controlled source. When programmed as an input, the N1225A board uses this pin to drive the internal clock line of the board. This allows multiple N1225A boards to be synchronized to a single 10 MHz source. See Figure 26 on page 77 for the clock logic.

~Sample1 to ~Sample4 Input/Output Pins

As inputs, these pins allow external hardware to latch the current value of the Position Counter into Position and Velocity registers for transfer over VMEbus. The signal on a ~Sample1 to ~Sample4 input causes the bits of the Position Counter to be latched into the correspondingly numbered Position 1 to Position 4 register shown in Figure 20. This occurs at the positive-going clock transition immediately following the high-to-low transition on the corresponding ~Sample input. The ~Sample1 and ~Sample2 inputs may also be programmed via the Hardware Sample Mode 0 and Hardware Sample Mode 1 bits of the General Control & Status register to simultaneously sample the Velocity 1 and Velocity 2 registers respectively.

Writing to one or more of the Drive Sample1 to Drive Sample4 bits of the Command register, causes the corresponding pin to become an output and to drive a ~Sample (active low) signal out on the P2 connector synchronous with the next 10 MHz clock edge.

Hardware Position Output

The P2 rows A and C are also used by the N1225A board to provide the Hardware Position output. The pins associated with this function provide access to the two Hardware Position registers shown in Figure 20 on page 57 as well as to the monitor and control functions described in the pin description sections below.

P0 to P35 Output Pins

P0 to P35 is a 36-bit, real time 3-state position output bus which, enabled by the ~Read pin of P2, will provide the value from the Hardware Position register to the output. This value will be provided if the address on the A0–A5 pins of P2 matches the Output Control register P2 A0 to P2 A5 bits programmed for that axis channel.

Error Output Pin

The Error signal is a status output that can be programmed via the P2 Error Mask register to indicate the presence of multiple error indicators. This output can be programmed via the Output Control register to operate as an open collector, TTL, or 3-state output by setting the configuration with the Error Mode Sel0 to Sel2 bits. It is enabled by the ~Read pin qualified by the A0–A5 pins of P2.

Force Zero Input Pin

The Force Zero pin, when pulled low, forces the 36 output lines (P0-P35) to zero.

~Position Reset Input Pin

The ~Position Reset pin, when pulled low, causes the Position Counter to either be zeroed or set to the value in the Position Offset register, depending on the state of the Preset Enable bit in the General Control and Status register.

Output Hold Input/Output Pin

The Output Hold pin, when pulled high, causes all four 36-bit Hardware Position registers shown in Figure 20 on page 57 to hold their current values.

The Agilent N1225A board can also be programmed via the Output Control register to drive the output hold I/O pin two ways:

- By using the AOH/OCLK line as an asynchronous hold input. Here the user drives the AOH/OCLK pin which then causes the Output Hold line to be driven by the N1225A synchronously with its 10 MHz clock.
- By using the internal divide-by-N feature. In this mode, the N1225A board "unloads" for one 100 ns period every N 100 ns periods, where N is programmed to be 1 through 64. Several N1225A boards can be tied together in this mode with one N1225A board programmed as the "master". This provides multi-axis synchronous output rates between 156.25 kHz and 10 MHz.

~Read Input Pin

The ~Read input enables the 36-position output lines P0 to P35 and possibly the Error pin, if and only if, the signal logic levels of the A0 to A5 pins of P2 match the value loaded into the P2 A0 to A5 address bits of the Output Control register. When the ~Read pin is pulled low, the P0 to P35 output pins of P2 are enabled. When ~Read is high, the output pins will be in a high impedance state. The P2 Error output line will also be enabled by the ~Read pin if it is programmed in the 3-state mode via the Output Control register.

AOH/OCLK Input/Output Pin

The AOH/OCLK pin is programmed via the Output Control register to operate either as an asynchronous output hold input or as a position output clock. When programmed as an asynchronous output hold input (Async Mode 1), an asynchronous hold signal may be applied, and the Hardware Position register bits will be guaranteed stable and held within 100 ns of this input going high.

When programmed as an output clock (Async Mode 2 or Async Mode 3), the Hardware Position register bits can be latched into your register on the rising edge of the AOH/OCLK signal.

A0 to A5 Input Pins

The A0–A5 address inputs are used as qualifiers for the ~Read input. The logic levels of the A0-A5 pins must match the value of the P2 A0 to A5 address bits in the Output Control register in order for the ~Read pin to enable the P0 to P35 data outputs of a particular board and axis channel.

These pins also enable the Error pin with the axis selected in the same way as above.

Overview for P2 rows D and Z

The N1225A P2 D and Z rows provide hardware I/O for developers needing faster data output, and hardware signals for Axis errors and Comparator outputs. Input pins are also provided to reset individual axes. Developers who are not using any of these features can use a backplane with three row connectors. All board power is supplied through the A, B, and C rows.

High speed parallel outputs

For each axis, ten pins on the P2 connector are dedicated to providing parallel position data words updated every 100 ns. Axis 1 is on the A and C rows and uses pins AxisX_P0 through AxisX_P9.

All four data outputs are turned on by setting bit D4, the all axes high speed data outputs enable bit in the Axis1 Setup Register. When the high speed outputs are enabled it is not possible to read the 36-bit position data, AxisX_P0 through AxisX_P35. By default, the high speed parallel outputs are off when the board is powered up. Data bits are synchronized with the 10 MHz clock with timing described in Chapter 8, “Specifications.”

Axis1 through Axis4 err out

These are TTL signals that are the ORed combination of the error conditions monitored by the board level error status and reset register ANDed with bits in the respective axis P2 error mask register. The signals remain active until the error condition is cleared and the bit in the board level error status and reset register is reset.

For example, the Axis1 err out line at P2–D17 will go high if the Axis1 data not valid bit, B0 in the Board level error status and reset register, goes high and the corresponding bit in the Axis1 P2 error status and reset register is set. Setting multiple bits in an axes P2 error mask register causes the respective axis error line to become active for multiple errors. These bits are not addressed.

Axis1 through Axis4 comp out

These are TTL active high signals that indicate the result of comparisons programmed by setting comparison logic in the “AxisX comparator configuration register” and limit values in the respective “AxisX position comparator high” and “low” registers. These bits are real time and updated at a 10 MHz rate.

~Axis1 reset in through ~Axis4 reset in

These are TTL active low signals. Bringing one of these lines low causes the value in the Position counter for that axis to be reset to zero or to the preset value, provided these inputs have been enabled by setting the AxisX D row reset enable bit in the AxisX setup register. If AxisX preset enable bit in the axis General control and status register is set, the value in the AxisX preset register is loaded into the axes position counter, otherwise, the position counter is zeroed.

Table 10 P2 A & C Row Drivers/Receivers/Terminations

	Driver/Receiver Chip	I_{ih} (mA max)	I_{il} (mA max)	I_{oh} (mA max)	I_{ol} (mA max)	Termination needed?
P0–P35 Outputs	74LVT245	—	—	–32	32	No[1]
External Measure and Reference Inputs	N/A	N/A	N/A	N/A	N/A	N/A
Error Output	74LVTH125	—	—	–32	32	No[1]
Window Output	N/A	N/A	N/A	N/A	N/A	N/A
Force Zero Input	74LVTH125	0.001	–0.005	—	—	No[1]
~Sample 1–4 I/O	74LVTH125	0.001	–0.005	–32	32	No[1]
~Position Reset Input	74LVTH125	0.001	–0.005	—	—	No[1]
Output Hold I/O	74LVTH125	0.001	–0.005	–32	32	No[1]
~Read Input	74LVTH125	0.001	–0.005	—	—	No[1]
10 MHz Clock I/O	74LVTH125	0.001	–0.005	–32	32	Yes
AOH/OCLK I/O	74LVTH125	0.001	–0.005	–32	32	Yes
A0–A5 Inputs	74LVT245	0.02	–0.005	—	—	Yes

[1] It can be terminated by 300Ω to +5V and 470Ω to ground.

NOTE

The following pins, connected to the 74LVTH125 parts, when used as inputs must be driven or have pull-up resistors, 6.6 kΩ maximum, to ensure a minimum current to the pin of 0.5 mA: Force Zero Input, ~Sample1-4, ~Position Reset, Output Hold, ~Read Input, AOH/CLK I/O. If this is not done the input logic state is unknown.

All inputs on the P2 row Z, if used, must be driven or have pull-up resistors, 6.6 kΩ maximum.

Table 11 P2 D & Z Row Drivers/Receivers/Terminations

pin #	Z Row		D Row	
	Driver/Receiver	Termination	Driver/Receiver	Termination
1	74LVT245	VME	74LVT245	VME
2	GND		74LVT245	VME
3	74LVT245	VME	74LVT245	VME
4	GND		74LVT245	VME
5	74LVT245	VME	74LVT245	VME
6	GND		74LVT245	VME
7	74LVT245	VME	74LVT245	VME
8	GND		74LVT245	VME
9	74LVT245	VME	74LVT245	VME
10	GND		74LVT245	VME
11	74LVT245	VME	74LVT245	VME
12	GND		74LVT245	VME
13	74LVT245	VME	74LVT245	VME
14	GND		74LVT245	VME
15	74LVT245	VME	74LVT245	VME
16	GND		74LVT245	VME
17	74LVT245	VME	74LVT245	VME
18	GND		74LVT245	VME
19	74LVT245	VME	74LVT245	VME
20	GND		74LVT245	VME
21	74LVT245	VME	74LVT245	VME
22	GND		74LVT245	VME
23	74LVT245	VME	74LVT245	VME
24	GND		74LVT245	VME
25	74LVT245	VME	74LVT245	VME
26	GND		74LVT245	VME
27	74LVT245	VME	74LVT245	VME
28	GND		74LVT245	VME
29	74LVT245	VME	74LVT245	VME
30	GND		74LVT245	VME
31	74LVT245	VME	GND	
32	GND		+5V	

N1225A Mechanical

The N1225A is a single width, 6U size board with five row connectors for P1 and P2. The basic overall dimensions with the injector/ejector handles in the open, as well as the locked position are shown in Figure 46. The injector/ejector handles provide leverage for inserting and removing the board from IEEE 1101.10 compatible card cages. The locking feature of these handles makes the use of front panel screws unnecessary. The N1225A has an alignment pin and three keying chambers in each injector/ejector handle. Refer to IEEE 1101.10 for information on the keying chambers.

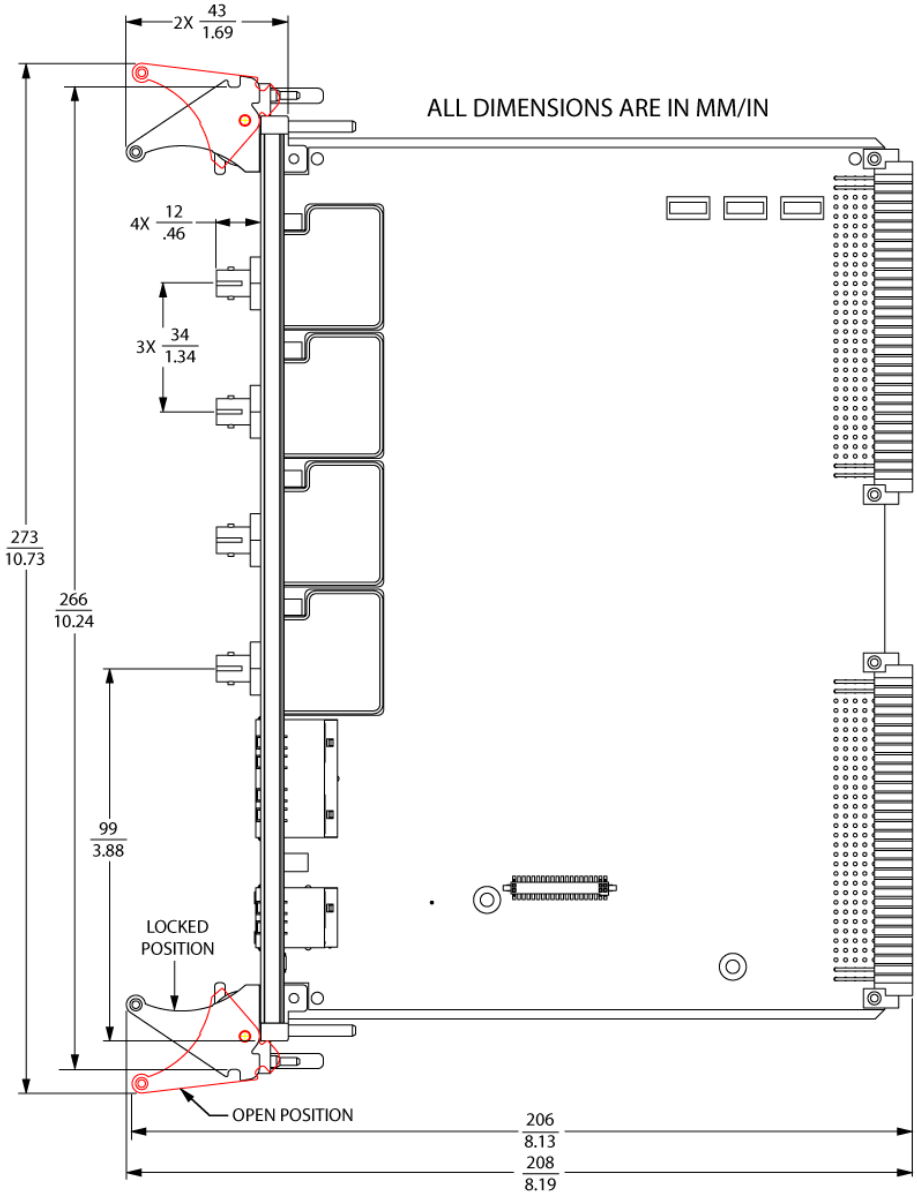


Figure 46 N1225A mechanical

The reference passing cable is long enough to allow one blank slot between boards.

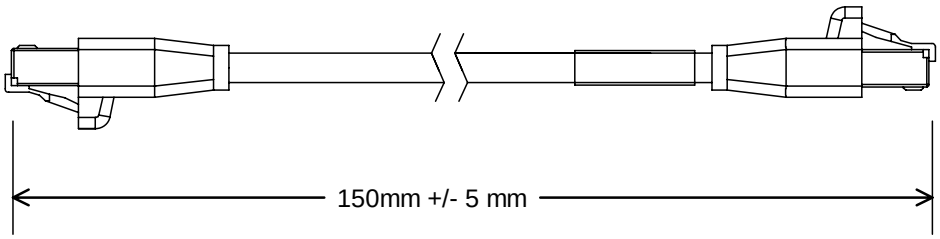


Figure 47 N1225-002 reference passing cable

6 Applications

Introduction

This chapter shows how the N1225A is configured and used in some common applications. The chapter includes sections on basic, intermediate and advanced applications. A section dedicated to multi-board setups is also included. A basic application will use only the web interface to communicate with a single laser axis board. An intermediate application communicates with one or more laser axis board using the VMEbus. An advanced application uses one or more laser axis boards, the VMEbus for communications, and collects data off the outer rows of the P2 connector.

The main focus of this chapter is on the electronics and it is assumed the optics are already set up, and good optical signals are available. For help with measurement setups and accuracy considerations, refer to the *Agilent Technologies Laser and Optics User's Manual* (part number 05517-90086) or CD version (05517-13602).

Basic Application

Description

This basic application uses the LAN exclusively to communicate with the laser axis board. You will need Sun Java VM installed to communicate with the board. In Figure 48 on page 200 there is a single axis application where the distance between the interferometer and plane mirror is measured by the N1225A. The laser system makes a relative position measurement, from the last time position was reset to zero or preset to another starting value.

Setup

If you do not know the IP address of the board, write down the board serial number and MAC address. The serial number is in the format "`US00000000`" and located by channel 1 on the component side. The MAC address is on the circuit side near P1 and P2 and has the format "`00:30:D3:00:00:00`".

If the board is just out of the box or if the reset button has been used to restore the factory default settings, then there are no more setup steps, because the following default axis configurations are already set up:

- Axis1 is defined as the phase of channel 1 minus the phase of channel 4.
- Axis2 is channel 2 minus channel 4.
- Axis3 is channel 3 minus channel 4.
- Axis4 is channel 4 minus channel 4, or zero.

Use

With the cables routed as shown in Figure 48 on page 200, apply +5V to the backplane and observe the status LED which will start blinking. After less than 30 seconds, the LED will be solid green. At this time, establish communications with the board over the LAN. If needed, refer to the power up and verification procedure in the maintenance and service chapter for help.

Once you can see the web page for the laser axis board, click on the various tabs to view what is available over the web. Browse through the web page to see the position readout for Axis1. Try viewing, but not changing some of the register contents using the basic interface described in the operations chapter.

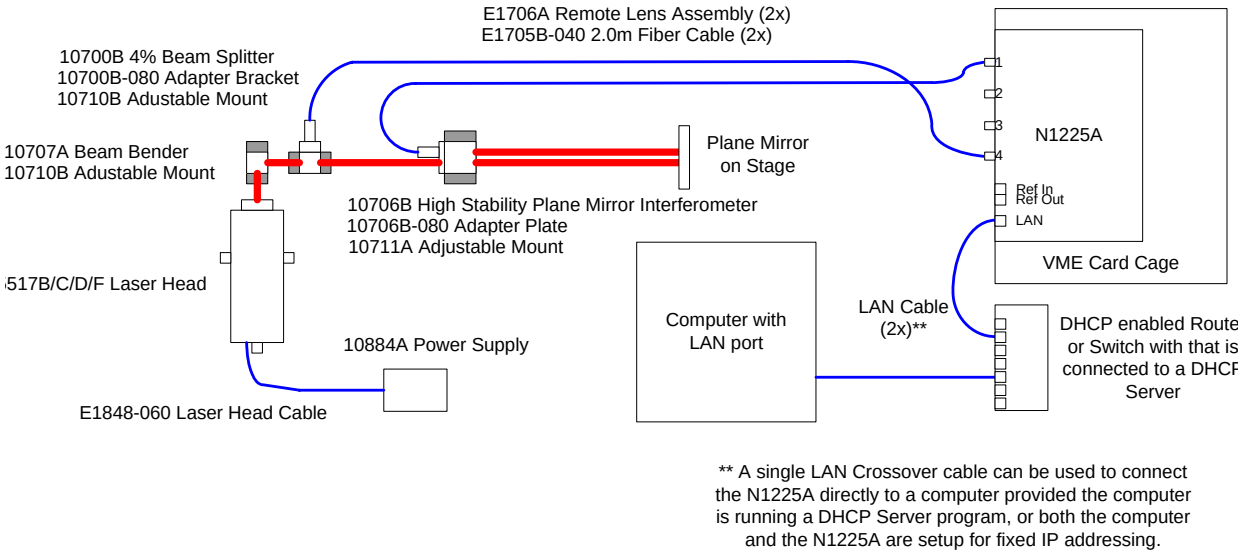


Figure 48 Diagram of a basic application

Intermediate Application

Description

The intermediate application uses the VMEbus for communications and requires writing or having a program to run on your VMEbus controller to communicate with the board. A simple application that allows reads and writes is enough. Figure 49 shows this application where six axes are being measured using two laser axis boards with a reference passing cable bringing reference data from board #1 to board #2.

Setup

1 Set the VME base address and addressing mode., either A16, A24, or GAP for board #1 and board #2,

2 Record the setting.

3 If you will be using the web interface, also record the serial number and MAC address if you do not know the IP address of the laser axis board. The serial number is in the format "`US00000000`" and located by channel 1 on the component side. The MAC address is on the circuit side near P1 and P2 and has the format "`00:30:D3:00:00:00`".

4 Assuming the board registers are in an unknown state, write the following values to these registers to set up the board for a normal configuration.

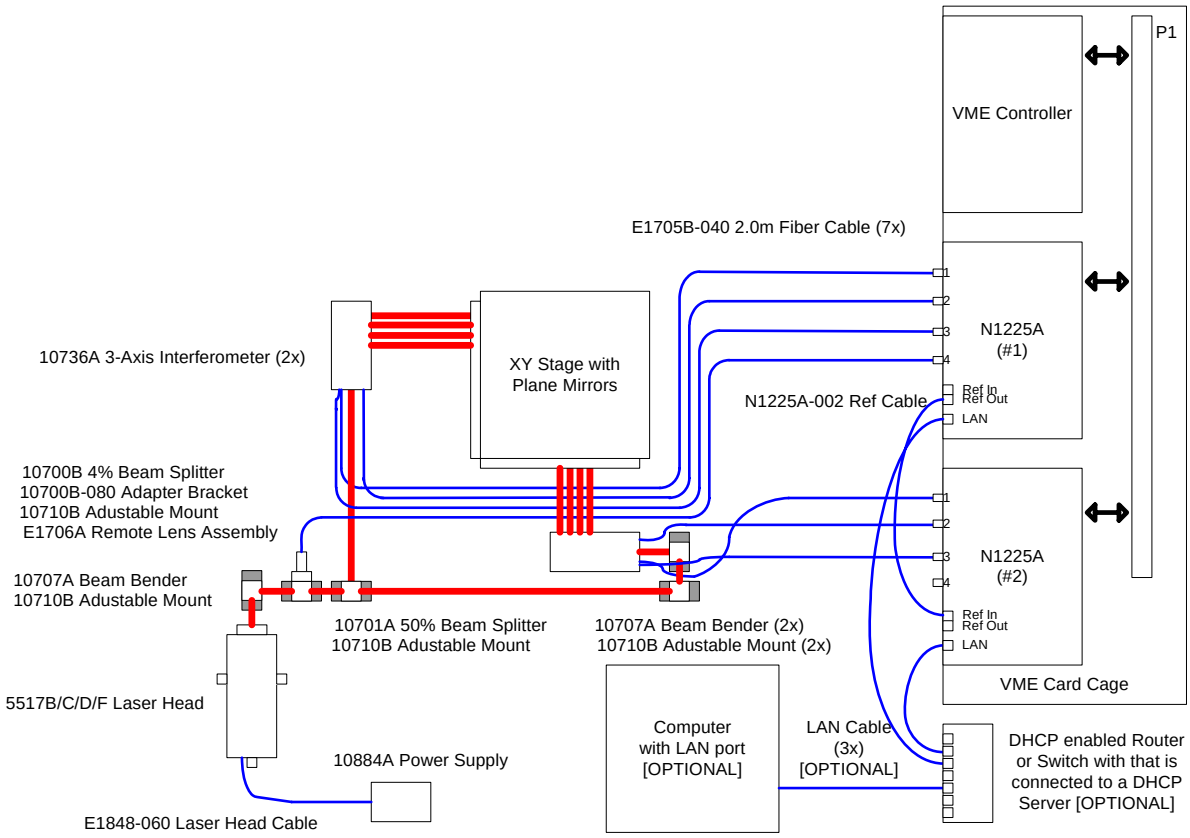


Figure 49 Diagram of an intermediate application

Table 12 Register Settings

OffsetS	Size	Register Name	Board 1	Board 2	Operation
0x0002	word	Axis 1 Status & Control	0x0020	0x0020	setup for ~Sample2 to sample Position & Velocity
0x0202	word	Axis 2 Status & Control	0x0000	0x0000	
0x0402	word	Axis 3 Status & Control	0x0000	0x0000	
0x0602	word	Axis 4 Status & Control	0x0000	0x0000	
0x0006	word	Axis 1 Source Control	0x0003	0x0004	setup for bd 1 channel 4 to be ref
0x0206	word	Axis 2 Source Control	0x0010	0x0010	setup for differential measurement with optical channel 1
0x0406	word	Axis 3 Source Control	0x0020	0x0020	setup for differential measurement with optical channel 1
0x0606	word	Axis 4 Source Control	0x0033	0x0034	
0x001C	long	Axis 1 gain and squelch	0x00000000	0x00000000	turn on AGC, turn off squelch

Table 12 Register Settings

OffsetS	Size	Register Name	Board 1	Board 2	Operation
0x021C	long	Axis 2 gain and squelch	0x00000000	0x00000000	
0x041C	long	Axis 3 gain and squelch	0x00000000	0x00000000	
0x061C	long	Axis 4 gain and squelch	0x00000000	0x00000000	
0x0026	word	Axis 1 Setup	0x0000	0x0000	setup for lsb = 0.15nm with pm optics
0x0226	word	Axis 2 Setup	0x0000	0x0000	
0x0426	word	Axis 3 Setup	0x0000	0x0000	
0x0626	word	Axis 4 Setup	0x0000	0x0000	
0x0098	word	Axis 1 Sample Delay	0x00FF	0x00FF	set to low sample delay (higher data age), ready for auto-sample
0x0298	word	Axis 2 Sample Delay	0x00FF	0x00FF	
0x0498	word	Axis 3 Sample Delay	0x00FF	0x00FF	
0x0698	word	Axis 4 Sample Delay	0x00FF	0x00FF	
0x009C	word	Axis 1 Sample Mode and Mask	0x0400	0x0400	setup for sample-read handshaking on pos3 only
0x029C	word	Axis 2 Sample Mode and Mask	0x0400	0x0400	
0x049C	word	Axis 3 Sample Mode and Mask	0x0400	0x0400	
0x069C	word	Axis 4 Sample Mode and Mask	0x0400	0x0400	
0x00A4	long	IRQ Mask Register	0x0000	0x0000	disable any interrupts
0x0028	long	Error Status And Reset	0xFFFFFFFF	0xFFFFFFFF	clear any errors
0x000C	word	Axis 1 Command Register	0x0100	0x0100	Reset position
0x020C	word	Axis 2 Command Register	0x0100	0x0100	
0x040C	word	Axis 3 Command Register	0x0100	0x0100	
0x060C	word	Axis 4 Command Register	0x0100	0x0100	

Use

Clear errors on all the boards by either writing `0xFFFF` to the Board Level Error and Status Register (BLSR), or by reading the BLSR and then writing 1s to clear the existing errors. This is easily done by reading, then writing the BLSR contents back to it. Temporarily saving the BLSR value can help during troubleshooting. Issuing a blanket “clear” by writing all 1s, can make the system work, but will also obscure what caused it to start working.

See Table 13 for the additional reads and writes required to accomplish the listed tasks. Note that these all assume the setup operations in Table 12 were already done.

Table 13 Register Settings

Offset	Size	Register Name	Write Values		Operation
			Board 1	Board 2	
Flash the Status LED					
0x0002	word	Axis 1 Status & Control	A = read	B = read	read present value
0x0002	word	Axis 1 Status & Control	A | 0x0080	B | 0x0080	Start flashing the Status LED
Stop Flashing the Status LED					
0x0002	word	Axis 1 Status & Control	A = read	B = read	read present value
0x0002	word	Axis 1 Status & Control	A & ~0x0080	B & ~0x0080	Stop flashing the Status LED
Set the Squelch Value					
0x001E	word	Axis 1 Squelch	0xNNNN	0xNNNN	Set the Squelch Value to 0xNNNN
0x021E	word	Axis 2 Squelch	0xNNNN	0xNNNN	
0x041E	word	Axis 3 Squelch	0xNNNN	0xNNNN	
0x061E	word	Axis 4 Squelch	0xNNNN	0xNNNN	
Read the Power Levels					
0x0014	long	Axis 1 AC & DC Power Level	read	read	Read AC and DC Power Levels
0x0214	long	Axis 2 AC & DC Power Level	read	read	AC = value >> 16 DC = value & 0x0000FFFF
0x0414	long	Axis 3 AC & DC Power Level	read	read	
0x0614	long	Axis 4 AC & DC Power Level	read	read	
Simultaneous Board Reset					
0x00E	word	Axix 1 Command	0x4000	0x4000	Resets Position for All axes on a single board
Auto Sample the Position					
0x0160	long long	Axis 1 Pos5 Auto-Sample	read	read	Read Position with auto-sample
0x0360	long long	Axis 2 Pos5 Auto-Sample	read	read	(relies on Sample Delay bit for POS5 being set. See Table 12 on page 202)
0x0560	long long	Axis 3 Pos5 Auto-Sample	read	read	
0x0760	long long	Axis 4 Pos5 Auto-Sample	na	read	
Simultaneously Sample All Positions					
0x000C	word	Axis 1 Command Register	0x1000	0x1000	Sample Position on all axes on a board using ~Sample4*
0x0118	long long	Axis 1 Pos4	read	read	Read Position from above sample
0x0318	long long	Axis 2 Pos4	read	read	
0x0518	long long	Axis 3 Pos4	read	read	
0x0718	long long	Axis 4 Pos4	na	read	

Table 13 Register Settings

Offset	Size	Register Name	Write Values		Operation
			Board 1	Board 2	
Simultaneously Sample All Positions and Velocities					
0x000C	word	Axis 1 Command Register	0x0400	0x0400	Sample Position and Velocity on all axes on a board using ~Sample2*
0x0108	long long	Axis 1 Pos2	read	read	Read Position from above sample
0x0308	long long	Axis 2 Pos2	read	read	
0x0508	long long	Axis 3 Pos2	read	read	
0x0708	long long	Axis 4 Pos2	na	read	
0x0134	long	Axis 1 Vel2	read	read	Read Velocity from above sample
0x0334	long	Axis 2 Vel2	read	read	
0x0534	long	Axis 3 Vel2	read	read	
0x0734	long	Axis 4 Vel2	na	read	
Sample All Positions only if last Sample has been Read					
0x000C	word	Axis 1 Command Register	0x0800	0x0800	Sample Position on all axes on a board using ~Sample3*
0x0110	long long	Axis 1 Pos3	read	read	Read Position from above sample (must be read before next sample can happen)
0x0310	long long	Axis 2 Pos3	read	read	See the setup of the Sample Mode and Mask registers in "Sample Mode and Mask Registers" on page 157
0x0510	long long	Axis 3 Pos3	read	read	
0x0710	long long	Axis 4 Pos3	na	read	
Setup the board to generate an Interrupt on Errors					
0x0020	word	Interrupt Vector Register	0x000X	0x000Y	Set the boards' Interrupt Vectors to 0x0X and 0x0Y
0x00A4	long	IRQ Error Mask Register	0x000F000F	0x000F000F	Setup to generate interrupt if any loss of lock or invalid data errors detected
0x0002	word	Axis 1 Status & Control	A = read	B = read	read present value
0x0002	word	Axis 1 Status & Control	A | 0x0008 | N	B | 0x0008 | N	Enable the board to generate an IRQ at interrupt level N (N = 0 to 7).

*Assumes there is no Row A & C overlay on P2 bus.

Advanced application

Description

The advanced applications use the VMEbus and the outer rows of the P2 connector. While the intermediate and basic applications can have multiple boards, they are not able to simultaneously sample the position of a large numbers of axes. There will always be a delay as the computer sends the sample command to board after board. In the advanced applications, the A and C rows of multiple laser axis boards are bussed together, using either a custom backplane or by attaching an A and C row overlay to the backplane. Figure 50 on page 207 shows an application where 11 axes are being measured using three laser axis boards.

Setup

1 Set the VME base address and addressing mode, either A16, A24, or GAP, for boards #1, #2 and #3.

NOTE Setting the board that receives the reference channel to the highest VME address and having all addressing be "consecutive" allows the 11 axis channels to also be consecutive in the VME address space.

2 Record the setting.

3 If you will be using the web interface and you do not have the IP addresses of the board, then record the serial numbers and MAC addresses for all if the laser axis boards since you can only talk to the board the LAN cable is plugged into, not adjacent boards. The serial number is in the format “US00000000” and located by channel 1 on the component side. The MAC address is on the circuit side near P1 and P2 and has the format “00:30:D3:00:00:00”.

4 Assuming the board registers are in an unknown state, write the following values to these registers to set the board up in a normal configuration.

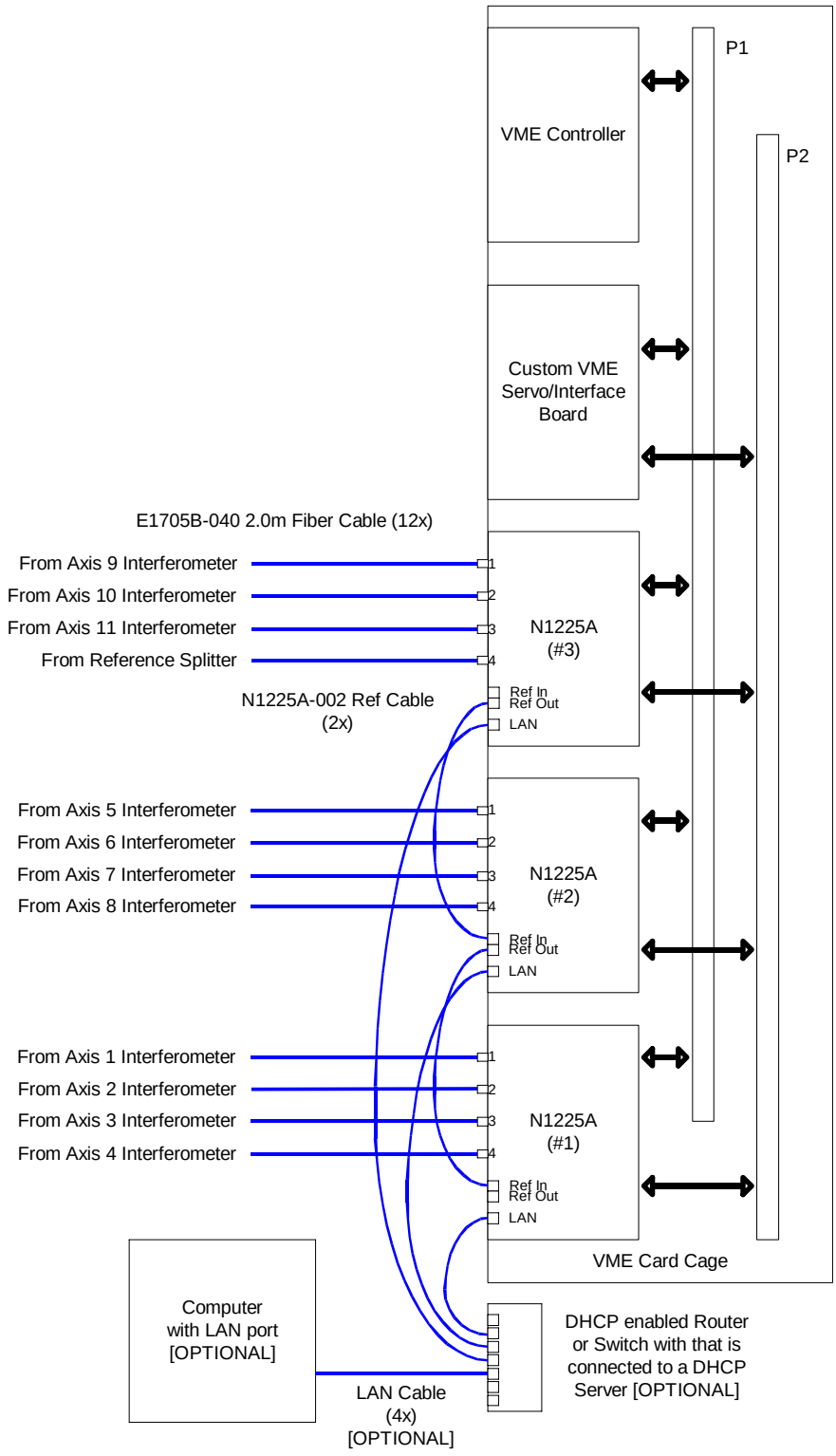


Figure 50 Diagram of an advanced application

Table 14 Register Settings

Offset	Size	Register Name	Board 1	Board 2	Board 3	Operation
0x0002	word	Axis 1 Status & Control	0x0020	0x0020	0x0020	setup for ~Sample2 to sample Position & Velocity
0x0202	word	Axis 2 Status & Control	0x0000	0x0000	0x0000	
0x0402	word	Axis 3 Status & Control	0x0000	0x0000	0x0000	
0x0602	word	Axis 4 Status & Control	0x0000	0x0000	0x0000	
0x0006	word	Axis 1 Source Control	0x0004	0x0004	0x0003	setup for bd 3 channel 4 to be ref
0x0206	word	Axis 2 Source Control	0x0014	0x0014	0x0013	
0x0406	word	Axis 3 Source Control	0x0024	0x0024	0x0023	
0x0606	word	Axis 4 Source Control	0x0034	0x0034	0x0033	
0x000A	word	Axis 1 Output Control	0x4000	0x4004	0xD008	setup: async mode 0 for boards 1&2 and mode 1 for bd 3, different P2 addresses, brd3 drives clock, common error line
0x020A	word	Axis 2 Output Control	0x0001	0x0005	0x0009	
0x040A	word	Axis 3 Output Control	0x0002	0x0006	0x000A	
0x060A	word	Axis 4 Output Control	0x0003	0x0007	0x000B	
0x00B4	word	Output Hold and Rate Control	0x0000	0x0000	0x0000	Do NOT drive output HOLD line with the clock divider output
0x001C	long	Axis 1 gain and squelch	0x00000000	0x00000000	0x00000000	turn on AGC, turn off squelch
0x021C	long	Axis 2 gain and squelch	0x00000000	0x00000000	0x00000000	
0x041C	long	Axis 3 gain and squelch	0x00000000	0x00000000	0x00000000	
0x061C	long	Axis 4 gain and squelch	0x00000000	0x00000000	0x00000000	
0x0026	word	Axis 1 Setup	0x0000	0x0000	0x0000	setup for lsb = 0.15nm with pm optics
0x0226	word	Axis 2 Setup	0x0000	0x0000	0x0000	
0x0426	word	Axis 3 Setup	0x0000	0x0000	0x0000	
0x0626	word	Axis 4 Setup	0x0000	0x0000	0x0000	
0x0098	word	Axis 1 Sample Delay	0x00FF	0x00FF	0x00FF	set to low sample delay (higher data age), ready for auto-sample
0x0298	word	Axis 2 Sample Delay	0x00FF	0x00FF	0x00FF	
0x0498	word	Axis 3 Sample Delay	0x00FF	0x00FF	0x00FF	
0x0698	word	Axis 4 Sample Delay	0x00FF	0x00FF	0x00FF	
0x009C	word	Axis 1 Sample Mode and Mask	0x0400	0x0400	0x0400	setup for sample-read handshaking on pos3 only
0x029C	word	Axis 2 Sample Mode and Mask	0x0400	0x0400	0x0400	

Table 14 Register Settings

Offset	Size	Register Name	Board 1	Board 2	Board 3	Operation
0x049C	word	Axis 3 Sample Mode and Mask	0x0400	0x0400	0x0400	
0x069C	word	Axis 4 Sample Mode and Mask	0x0400	0x0400	0x0400	
0x00A4	long	IRQ Mask Register	0x0000	0x0000	0x0000	disable any interrupts
0x0028	long	Error Status And Reset	0xFFFFFFFF	0xFFFFFFFF	0xFFFFFFFF	clear any errors
0x000C	word	Axis 1 Command Register	0x0100	0x0100	0x0100	Reset position
0x020C	word	Axis 2 Command Register	0x0100	0x0100	0x0100	
0x040C	word	Axis 3 Command Register	0x0100	0x0100	0x0100	
0x060C	word	Axis 4 Command Register	0x0100	0x0100	0x0100	

Use

See Table 15 for the additional reads and writes required to accomplish the listed tasks.

NOTE These all assume the setup operations in Table 14 were already done.

Table 15 Register Settings

Offset	Size	Register Name	Board 1	Board 2	Board 3	Operation
Simultaneous Board Reset						
0x000E	word	Axis 1 Command	0x4000	0x4000	0x4000	Resets Position for all axes on a single board
Simultaneously Sample All Positions						
0x000C	word	Axis 1 Command Register	na	na	0x1000	Sample Position on all axes on all boards using ~Sample4
0x0118	long long	Axis 1 Pos4	read	read	read	Read the values sampled above
0x0318	long long	Axis 2 Pos4	read	read	read	
0x0518	long long	Axis 3 Pos4	read	read	read	
0x0718	long long	Axis 4 Pos4	read	read	na	
Sample All Positions at Fixed Rate						
0x000A	word	Axis 1 Output Control	na	na	A = read	Setup to sample all boards at 500 kHz for output on the P2 bus

Table 15 Register Settings

Offset	Size	Register Name	Board 1	Board 2	Board 3	Operation
0x000A	word	Axis 1 Output Control	na	na	(A & ~0x3000) | 0x2000	(this relies on external hardware to co-ordinate outputting the data on P2, the AOH/OCLK line should be used to sync that equipment to the samples)
0x00B4	word	Output Hold and Rate Control	na	na	0x0093	
Setup to Generate Interrupt on External Sample						
0x0020	word	Interrupt Vector Register	na	na	0x000Z	Set board 3's Interrupt Vector to Z
0x069E	word	Axis 3 Sample Mode & Mask	na	na	A = read	read present value
0x069E	word	Axis 3 Sample Mode & Mask	na	na	A | 0x0001	Setup to generate interrupt when Sample1 occurs
0x0002	word	Axis 1 Status & Control	na	na	C = read	read present value
0x0002	word	Axis 1 Status & Control	na	na	C | 0x0008 | N	Enable the board to generate an IRQ at interrupt level N (N = 0 to 7).
Clear Interrupt and Read Positions in ISR						
0x06A2	word	Axis 3 Sample Status	na	na	read	Determine Interrupt Cause (verify Sample1 bit true)
0x0100	long long	Axis 1 Pos1	read	read	read	Read the values sampled by external input on ~Sample1 line
0x0300	long long	Axis 2 Pos1	read	read	read	
0x0500	long long	Axis 3 Pos1	read	read	read	Read of board 3, axis 3 clears this interrupt
0x0700	long long	Axis 4 Pos1	read	read	na	

Multi-Board Setup

VME Laser System Block Diagram

The Advanced Application shown in Figure 50 on page 207 shows all the boards connected to the P2 bus. And while Table 14 on page 208 lists the setup values for proper operation of the P2 bus, additional explanations for the Laser Source Control Registers and the Output Control Registers will help in adapting this particular configuration to other possible configurations.

Laser Source Control Register

The Source Control register needs non-default values for two situations. First, when multi-axis systems require taking the difference between two measurement signals. And second, when multi-board systems require using the same reference signal on more than one board.

For the multi-axis situation where one wants to measure pitch or yaw directly from the two measurement signals coming from a multi-axis optic (or two optics), the default reference signal selection must be changed from optical channel 4 to one of the other optical channels. Figure 49 on page 202 shows a six axis setup with two pitch and two yaw measurements. To get the pitch and yaw directly, the 2nd and 3rd axes for each board are setup to make a differential measurement by comparing their respective meas input signals against the axis 1 meas input signal instead of the optical reference on channel 4 or the passed electrical reference for board #2. See the Axis 2 and Axis 3 Source Control values for both boards in Table 12 on page 202.

For all multi-board applications the Ref Passing Cable, via the front-panel Ref IN and Ref OUT connectors, will be used to pass the reference signal from one board to the next. Figure 50 on page 207 shows an example of this for an eleven axis system. When using this cable the Source Control register must also be adjusted to select the electrical reference from an adjacent board as the reference input instead of optical channel 4. See the entries for the Source Control registers in Table 14 on page 208.

Output Control Register

The Clock Mode and Async Mode features become more important for multi-axis use. Figures 51 and 52 show examples of how to use these features.

Figure 51 provides an example of how to configure several laser axis boards so that one asynchronous hold input may be used to cause all of the 36-bit position outputs to hold on the same 10 MHz clock period. Simply connecting all of the AOH/OCLKs together will not insure this. See Figure 25 on page 73

and “Board Level Output Hold & Rate Control Register (32-Bit Offset $00B4)" on page 118 for more information. In the example shown, you assert the asynchronous hold input and access each 36-bit hardware position value, one by one, before releasing the hold input.

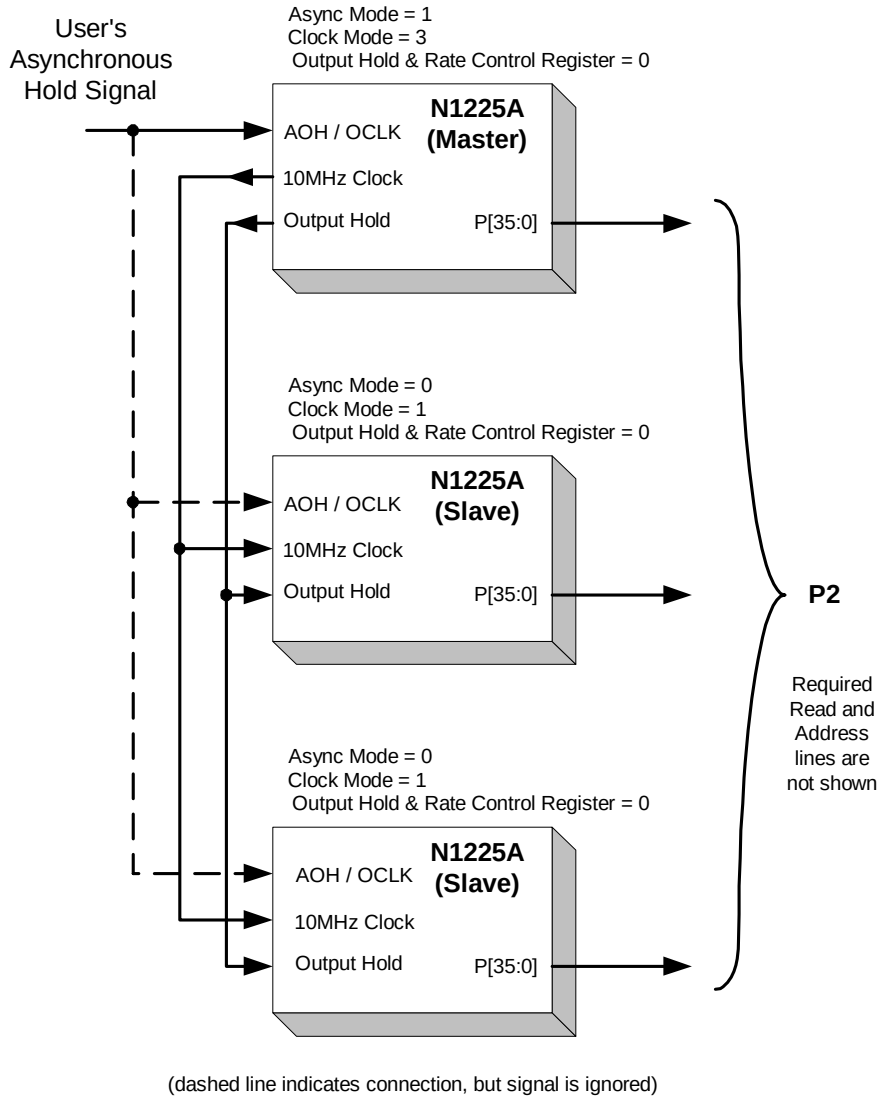


Figure 51 Asynchronous Hold Input for multi-board applications

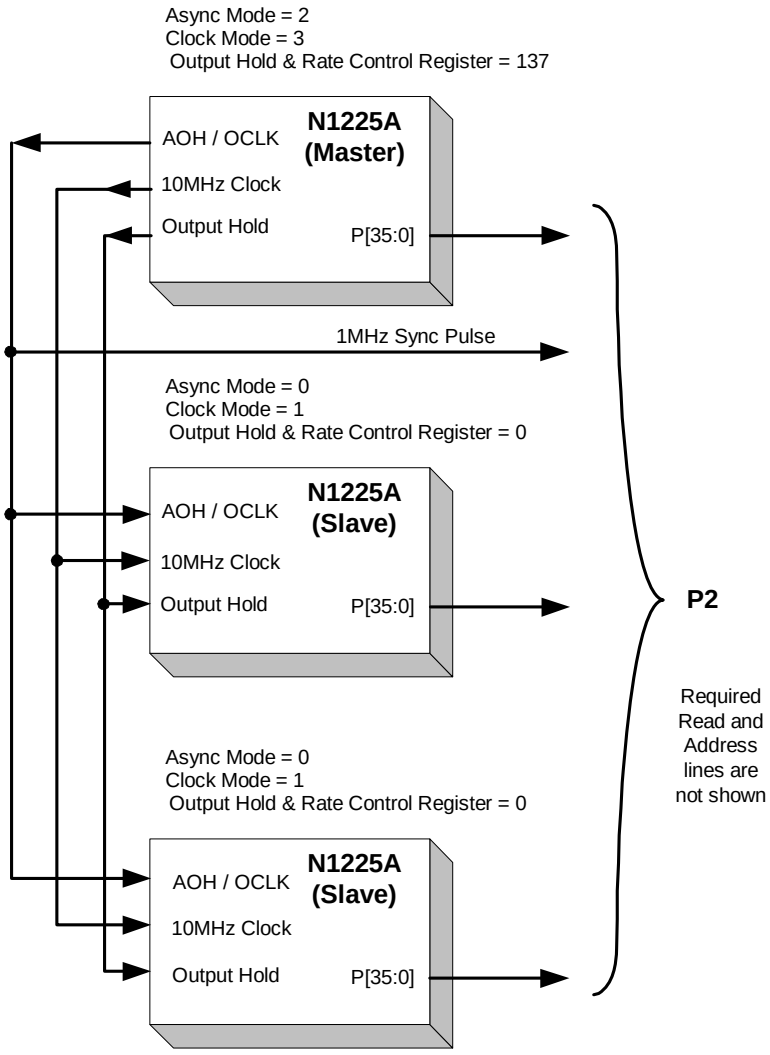


Figure 52 Synchronously latching for multi-board applications

Figure 52 provides an example of how to configure several laser axis boards so the P0-P35 hardware outputs may be synchronously read at the chosen rate of 1 MHz. Here the AOH/OCLK pin is configured as an output to initiate transferring the data over the P2 bus. With up to 11 axes in a 3-board system, the P2 address lines must change every 90 ns to read all 11 axes before the held values are updated. Setting the Output Hold and Rate Control register to the value of 9 sets the rate to 10 MHz ÷ (9+1) = 1 MHz. For more information, see Figure 25 on page 73 and "Board Level Output Hold & Rate Control Register (32-Bit Offset $00B4)" on page 118.

Setup Checklist

Because the user interface for the laser axis board is entirely through software, the only way to get the board working the first time, if the interface program does not already exist, is to write software and try basic functionality through the VMEbus. This can be a complicated process and things might go wrong at any step. To help you avoid some of these problems if you happen to be setting the board up for the first time, we have provided a short check list of essential items in roughly the order in which they would occur.

Once you get the VMEbus communication working, the laser axis board has some built-in diagnostics that will put signals through the board without requiring input signals. For details, see "Laser Source Control Register" on page 142.

To isolate specific problems, we have provided a troubleshooting section that answers some common questions. For details, see Chapter 7, "Maintenance and Service".

Agilent N1225A Setup Checklist

1 *Set the VMEbus address into S1 and S2*. If only one board is being set up, this address can be 0 with all switch positions down. If more than one board is present, each board must have a different address. For details, see "Installing the Board" on page 38.

2 *Set the A16/A24 and GAP switch position of S1 to match the kind of VMEbus address space that your software is using*. For details, see "Installing the Board" on page 38.

3 *In your software, initialize all registers of all four channels*. For details, see "Intermediate Application" on page 201 along with the matching information in Chapter 4, "Register Bit Descriptions.

4 *Verify that shared function setups are correct*. Generally the Axis 1 version of a register will contain some shared function setup bits. Make sure these are set properly since the overall value for axis 1 will be different than the setups for the other axes.

5 *Write to one of the control registers and then read the value back*. This will tell you quickly that your VMEbus interface is working.

6 *Try one of the operations given in Table 13* on page 204. Use an example that is close to your intended application. Once the example works, modify it to achieve the result you want.

7
Maintenance and Service

Introduction

This chapter provides maintenance and service information, including storage and shipment.

The Agilent N1225A requires no maintenance or calibration and, other than some cosmetic items, has no user serviceable parts. If a hardware failure occurs, contact the nearest Agilent Sales and Service office for return instructions.

Hazardous Voltages—When inserting, removing or handling the N1225A board, always use the injector/extractor handles and avoid touching the circuit board itself to avoid electric shock.

Areas of the N1225A circuit board near the front panel are energized with up to 180 Volts DC during board operation and this voltage can also be stored in board capacitors after power is removed and the board is turned off.

Safety first!

Before operating the N1225A, familiarize yourself with the safety markings on the instrument and the safety instructions in this manual. This instrument has been manufactured and tested according to international safety standards. To ensure safe operation of the instrument and the personal safety of the user and service personnel, the cautions and warnings in this manual must be heeded. Refer to the summary of safety considerations at the front of this manual.

Protect against ESD damage

Electrostatic discharge (ESD) can damage or destroy electronic components. All work should be performed at a static-free work station.

Storage and Shipment

To protect the board during storage or shipment, good anti-static commercial packing methods should be used. Reliable commercial packing and shipping companies have the facilities and materials to adequately repack a product.

Conditions during storage and shipment should normally be limited as follows:

- Minimum temperature: –40° C (–40° F).
- Maximum temperature: +75° C (+167° F).

Running the Diagnostics

To open the In Service Diagnostic Tests window

On the N1225A Welcome page, click the Diagnostics tab to open the In Service Diagnostic Tests screen.

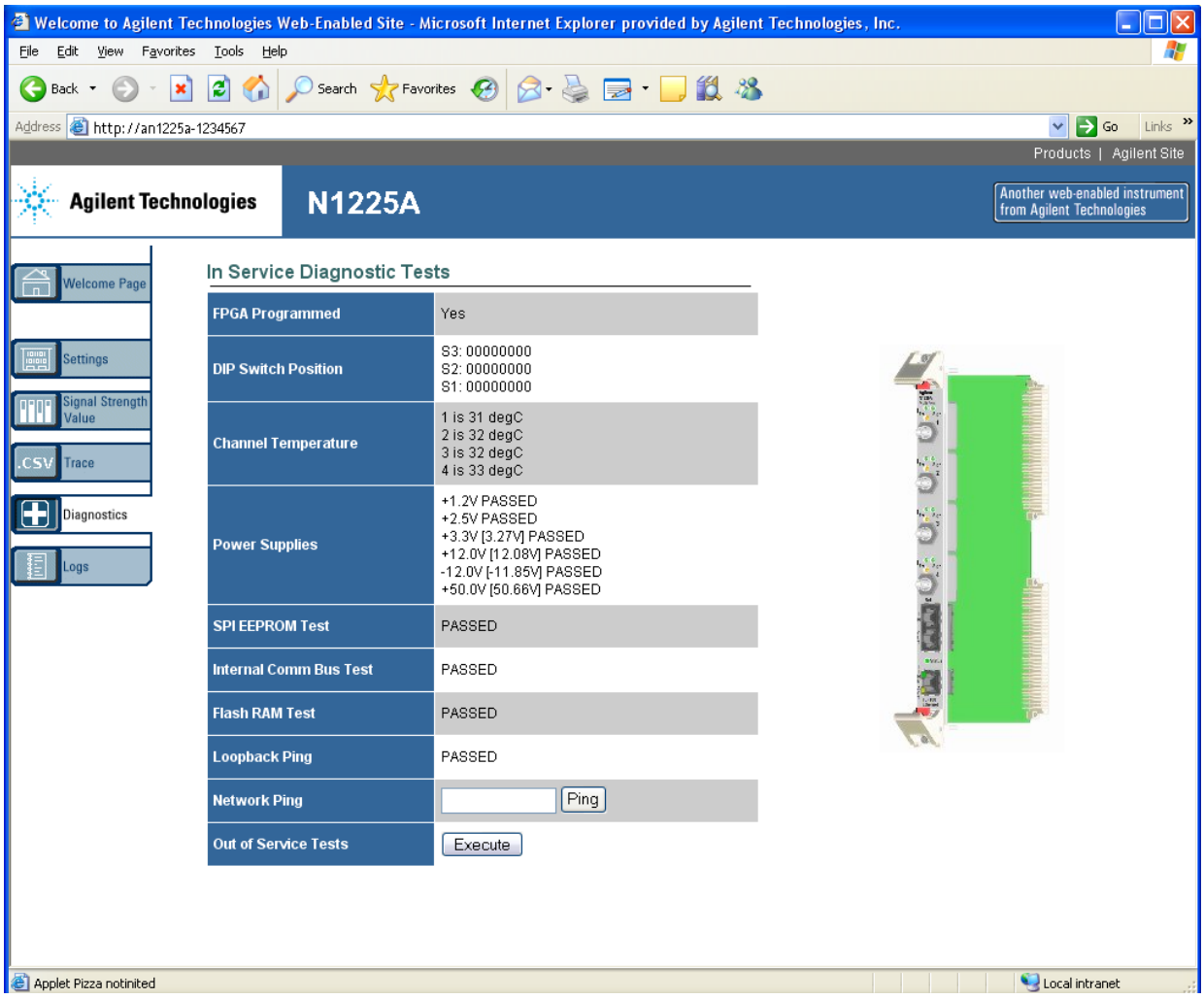


Figure 53 In Service Diagnostic Tests screen

This window shows the In Service Diagnostic tests and the current status for DIP Switch Position, Channel Temperature and Power Supply voltages.

Except for the network ping test these tests run every time the Diagnostics tab is clicked. They are called In Service Diagnostics Tests because they will not affect the data being read over VME or the P2 bus.The Out of Service Tests, however, will cause position to be lost on some or all axes, depending on which test is run.

In Service Diagnostic Tests selections

FPGA Programmed ***YES***
This test verifies the FPGA code was loaded without errors.

DIP Switch Position
S3: 00000000, S1 and S2 should reflect current settings.
A "0" means the switch handle is in the DOWN position. The switch closest to the front-panel corresponds to the first character in the field. See Figure 1 on page 21 and Figure 9 on page 39 for switch location. This is continually monitored.

Channel Temperature ***Below 55ºC***
Channel temperature is continuously monitored. A channel high temperature bit in each General Control and Status register will be set at 55º C and above.

Power Supplies ***All should show PASSED***
Power supply voltage status is available in the Board Level Diagnostics register and is continuously monitored.

SPI EEPROM Test ***PASSED***
This test verifies it is possible to read and write to the board EEPROM.

Internal Comm Bus Test ***PASSED***
This test checks the internal communications bus on the board.

Flash RAM Test ***PASSED***
This test checks the RAM.

Loopback Ping ***PASSED***
Result of testing the board by having it ping itself.

Network Ping
Run this test anytime to verify the board can reach another IP address. Enter the IP address and press the ping button.

Out of Service Tests
Press the Out of Services button to open a dialog box for proceeding to the Out of Service tests.

To open the Out of Service Diagnostic Tests panel

To open a open a dialog box for proceeding to the Out of Service tests press the Execute button next to Out of Services on the In Service Diagnostic Tests screen. A screen similar to the one in Figure 54 will open.

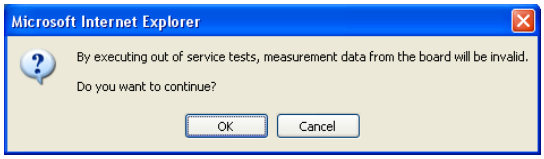


Figure 54 Out of Service Test dialog box

WARNING Running these tests can cause permanent loss of position data. They should not be run while the board is controlling a stage or taking important data.

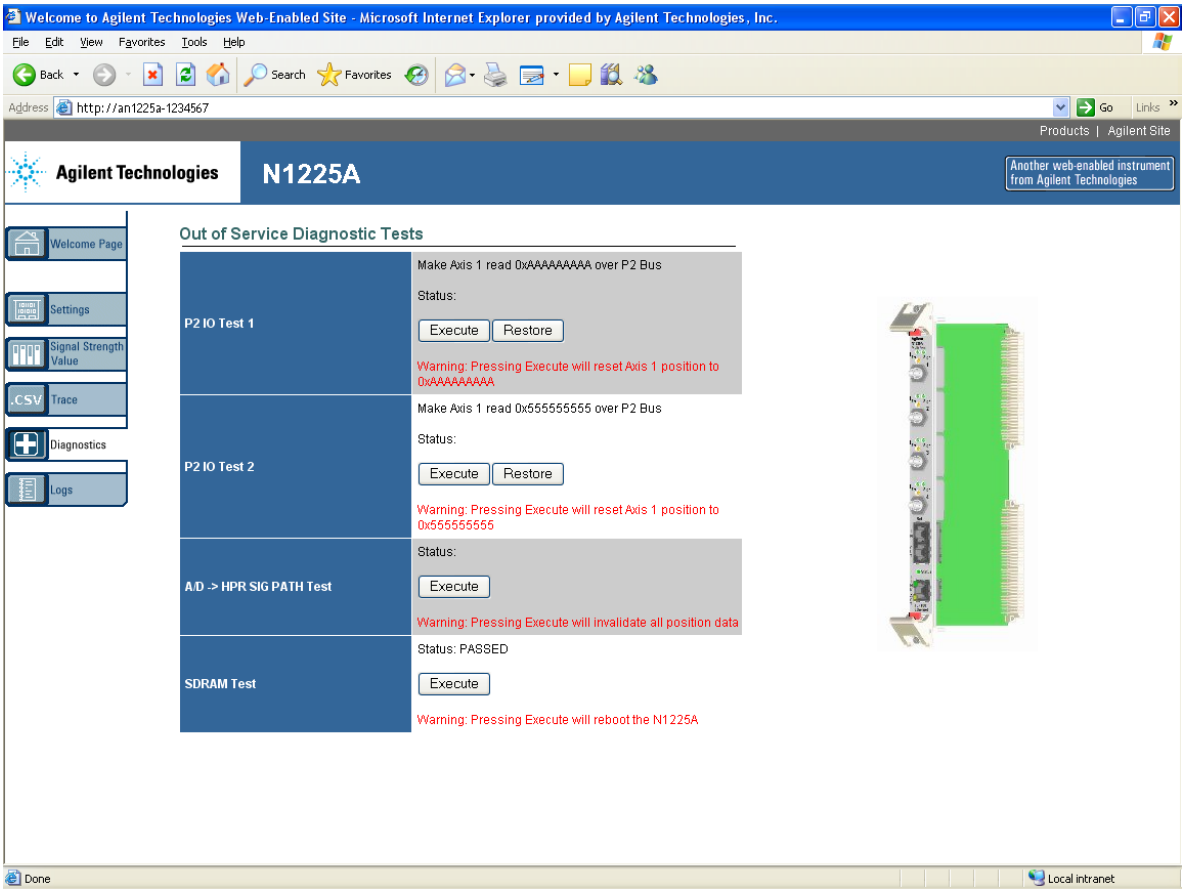


Figure 55 The Out of Services Diagnostic Test screen

Out of Service Diagnostic Tests panel

P2 IO Tests 1 and 2

These tests place a known, fixed value in the Axis 1 register to allow testing the ability of external hardware to read position data off the P2 user defined rows. Pressing Execute sets Axis 1 position to either “AAA...” or “555...” by changing the contents of the Laser Source Control Register for Axis 1 to 0x55, then presetting Axis 1 position. Once Execute is pressed, you should read the indicated values from the Axis 1 hardware position register over the P2 bus. After testing is complete, the original contents of the Laser Source Control Register are restored by pressing the Restore button. Axis 1 position will also be zeroed. If, however, you leave this Diagnostics page, then return, the Laser Source Control Register values *cannot* be restored.

A/D -> HPR SIG PATH Test ***PASSED***

A test signal is applied to the input of each channels A/D converter (see Figure 19 on page 56) while the output of each Hardware Position Register (see Figure 20 on page 57) is checked to verify the signal path integrity. *Position data for all axes is lost when this test is run.*

SDRAM Test ***PASSED***

For this test, Status: PASSED means the test passed when the board was powered up. Pressing Execute causes a complete board reboot, equivalent to turning the board power OFF and then ON. Stored values are not affected (DHCP ON/OFF, IP address (if static).

In Case of Difficulty

Problems upgrading the software

Board software can be upgraded, or downgraded, to previous revisions. Click the Upload button to copy the software from a file on your computer to the board. If the process goes through this step without an error, it should carry through to completion. If you are unable to communicate after upgrading the software, contact the local Agilent office.

Establishing communications over the LAN

First, verify your LAN is up and running by checking the green link LED labeled LINK. It should be on. Verify the amber activity LED labeled ACT is flashing to show data is traveling on the network, but not necessarily to your board. If the LAN configuration is unknown, refer to the Power Up and Verification Procedure, 40.

Communications over the VMEbus

When troubleshooting this problem, limit yourself, at first, to reading only known values such as the board MAC address and the board serial number. If you are reading unexpected values, the problem is often caused by inadvertently reading the wrong address.

Double check the settings of the N1225A address switches S1 and S2 using the installation information in Chapter 2. Also check the address switch settings for other boards in your system to make sure that two or more boards in the backplane do not have the same VME address.

If you are relying on GAP (Geographical Addressing Protocol) to set the board address, make sure GAP is enabled. To enable GAP the far left switch in S2 should be up.

Verify you are computing the address correctly by adding the address offset to the board base address which is set using S1 and S2.

Verify your reads are done on the proper word boundaries. If you are reading a 16-bit value, the address must be divisible by 2 and when reading a 32-bit value, the address must be divisible by 4. In *no* case should you be using an odd address. The N1225A does not support reading individual bytes.

To further troubleshoot, turn off the power to the rack and pull the other boards out of the backplane so only your controller and one N1225A board are plugged in. Set all N1225A switches in S1, S2 and S3 down. See Figure 2 on page 22. In this configuration, the board is in A16 addressing mode, with the board address set to hex $0000. Use your controller to perform a 16-bit read of address $0044, the MAC address register. You should get a hex value of $DC, base 10 value of 220, at this location. If this works, try restoring the N1225A board address to its original value, compute the register address and see if the same value can still be read.

Last, verify your controller can read other boards over the VMEbus or, if available, try using a different N1225A board.

Reading invalid data over the VMEbus

Verify the register address is being computed correctly. If you are reading a 32-bit register using 16-bit reads, remember data on the VMEbus is in “big endian” format, meaning the most significant 16-bits are in the lower address location and the least significant 16-bits are in the next address location. This is opposite of how data is stored in PC.

Reading invalid data over the P2 connector

Verify you are accessing the correct axis, keeping in mind the P2 bus has its own address bits (A0–A5) and is independent of the VMEbus. The value you put on A0–A5 (positive TTL logic) has to match the P2 axis address specified in the Output Control and Status Register for that axis when you bring the ~Read line low. Verify no two axes in your system have the same P2 bus address. Try setting channel phase to zero for the channels you are using by entering 55 for Meas A and Meas B in the Laser Source Control register. Then preset that axis to a known value and see if you can read that value on P2. If the value read is off by some factor of 2, verify the AxisX P2 bus bit alignment bits in the Output Control Register for that axis. See if the lsb selected there is what you want. By default, the lsb is 0.6 nm (plane mirror) to match the 10897/9 boards. If you have set a fixed position using 55 and by presetting as mentioned above, but data is changing, use a logic analyzer or oscilloscope to check timing.

Data on P2 A&C rows or D&Z rows not present

To avoid possible bus contention, the P2 outer row outputs are disabled when the board is powered up. Enable them by setting bits in the Setup registers

Symptoms of board overheating

The APD temperature value read from the Channel Status/Diagnostics register or the N1225A web page Diagnostics tab information indicates the temperature is over 55ºC. Any ChannelX high temperature bit, located in the General Control and Status Register, is set. The Data invalid bit, the Board Level Error Status and Reset register, is set and cannot be cleared because the high temperature shutdown has turned off high voltage to the APDs to reduce the chance of damage. This is not an all-inclusive list.

How to determine if a backplane driver IC is damaged

Put known, fixed values on the P2 bus, then toggle and check each bit. See Reading invalid data over the P2 connector, 223.

Value read from position register does not match preset value and is off by some factor of 2

The lsb for preset always has a resolution of 0.15 nm (plane mirror) whereas the resolution of the position registers is, by default, 0.6 nm until you change it. The Position register resolution is controlled by bits in the Setup registers.

Software and Firmware Upgrades

Agilent N1225A Firmware is upgradeable through a LAN port using a web browser to upload the new firmware. On the Agilent website, www.agilent.com, look up the N1225A for information on obtaining the firmware updates.

Using the following procedure, you can upgrade the Agilent N1225A in the field using the built-in LAN port and a PC to download new code. Information on the current revision of firmware is available on the Agilent web site by searching for “N1225A”.

Agilent N1225A software upgrade procedure

1 Establish communication with the N1225A via the LAN port.

2 From the Agilent N1225A Web Interface, select the *Settings* tab on the left hand side. The screen shown in Figure 56 should appear. Scroll down to the N1225A Firmware section where you will find the current Software Version and Hardware Version information installed in the product*.

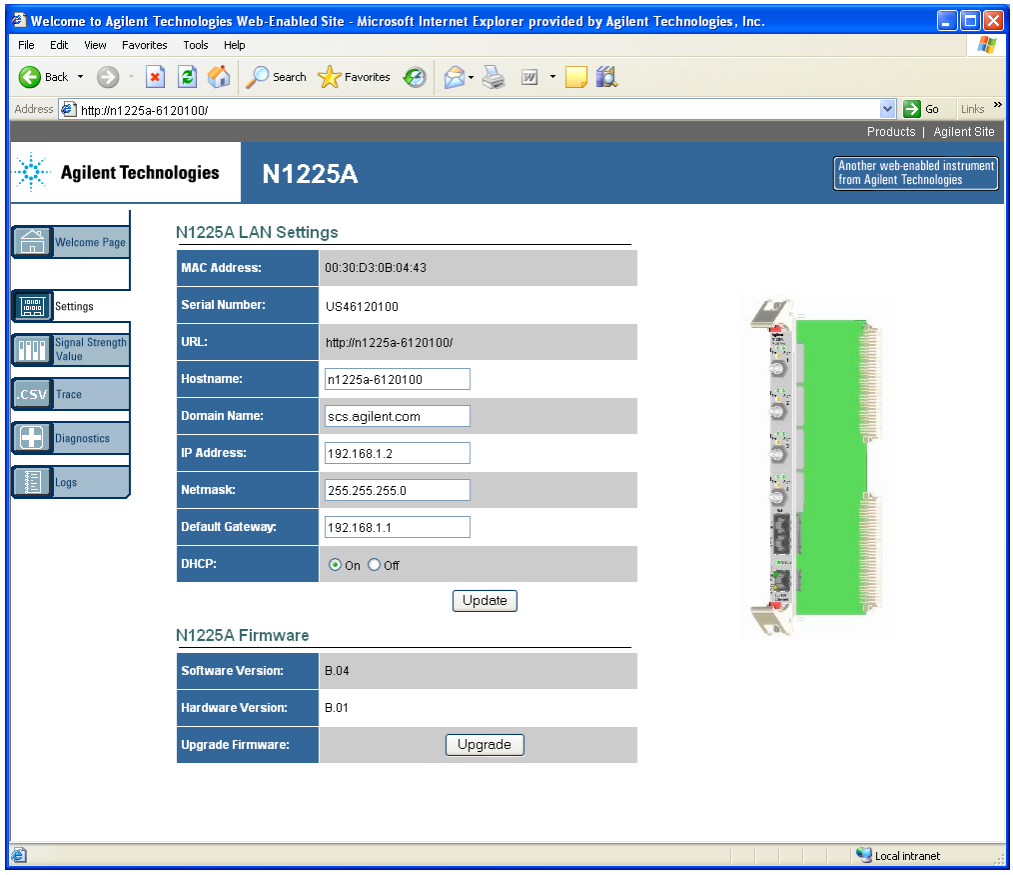


Figure 56 Firmware section of the Settings screen

* The Agilent website, www.Agilent.com, has information on the latest revision of the N1225A software.

3 To perform a software upgrade, click on the Upgrade button located on the bottom of the screen. You will see something similar to the screen in Figure 57.

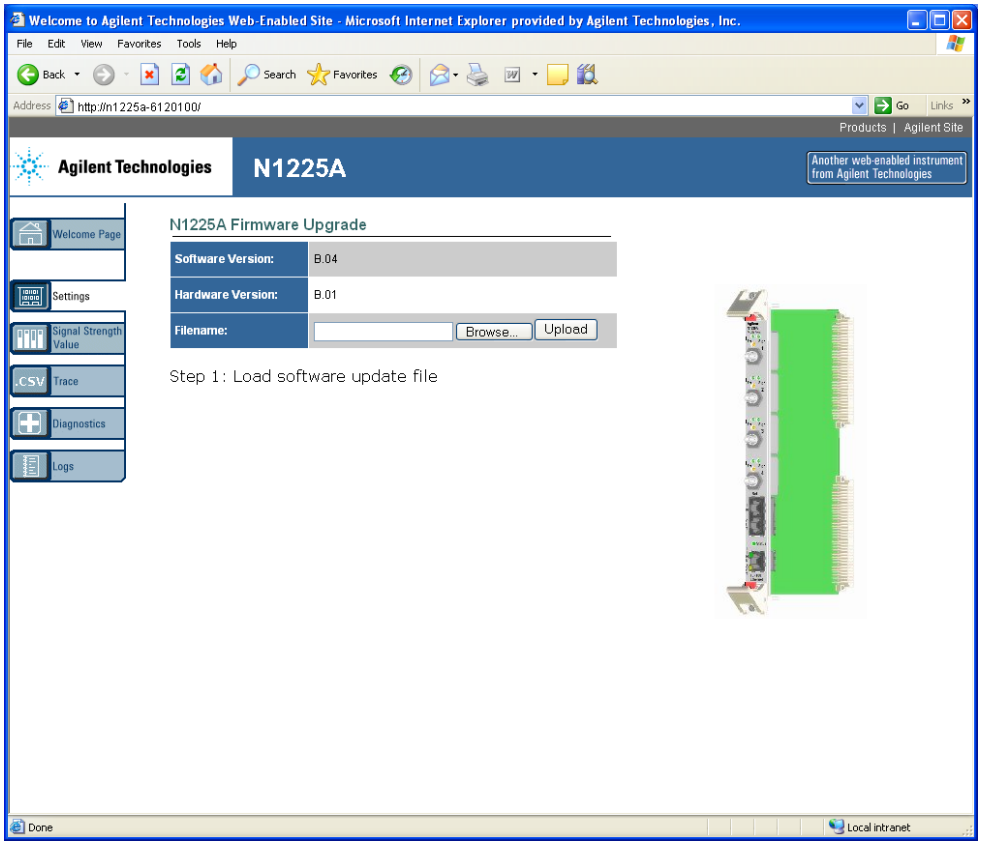


Figure 57 The Update screen

4 Next, click on the *Browse* button and locate the software update file. After selecting the file, the name of the file should appear in the Filename box. Click the *Upload* button to continue. After uploading the file, click on the *Program* button to begin the upgrade.

NOTE If you receive a CRC `Error` message, refresh the web page and try uploading again.

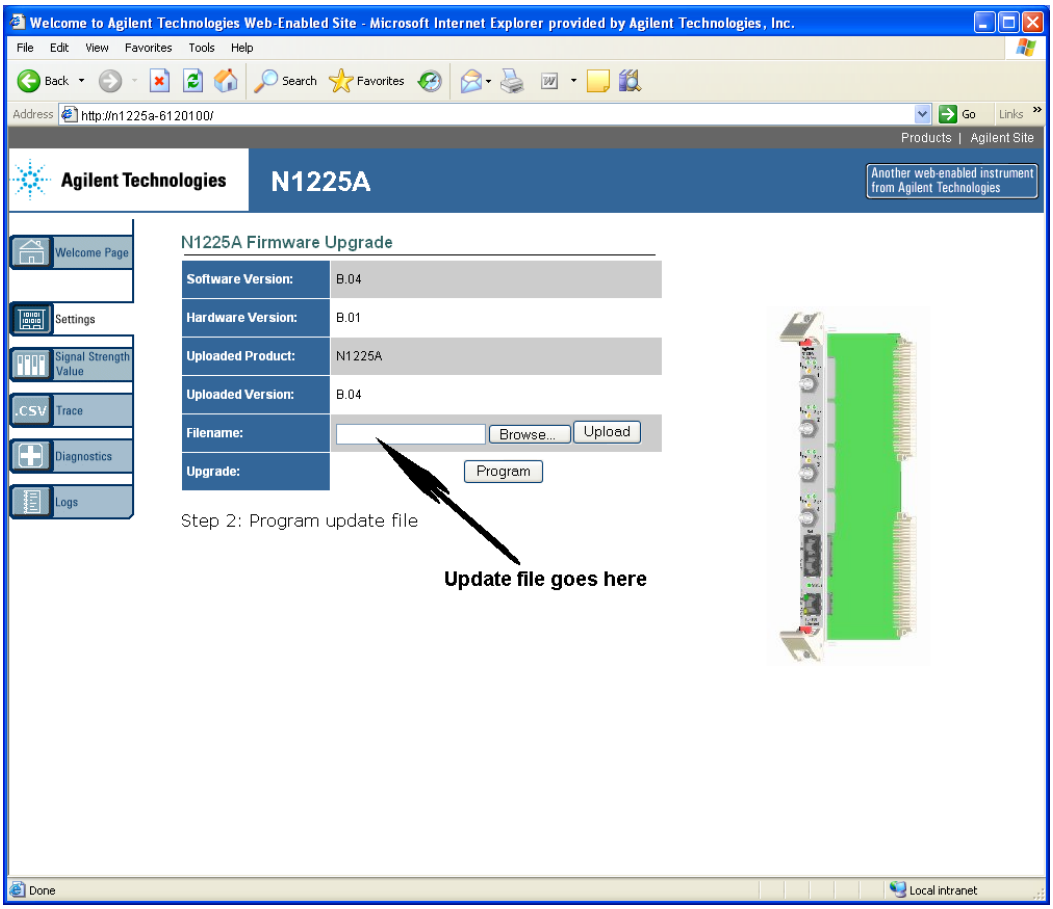


Figure 58 Upload the update

Once the upgrade gets underway, you will see a series of progress updates on your screen as shown in Figure 59.

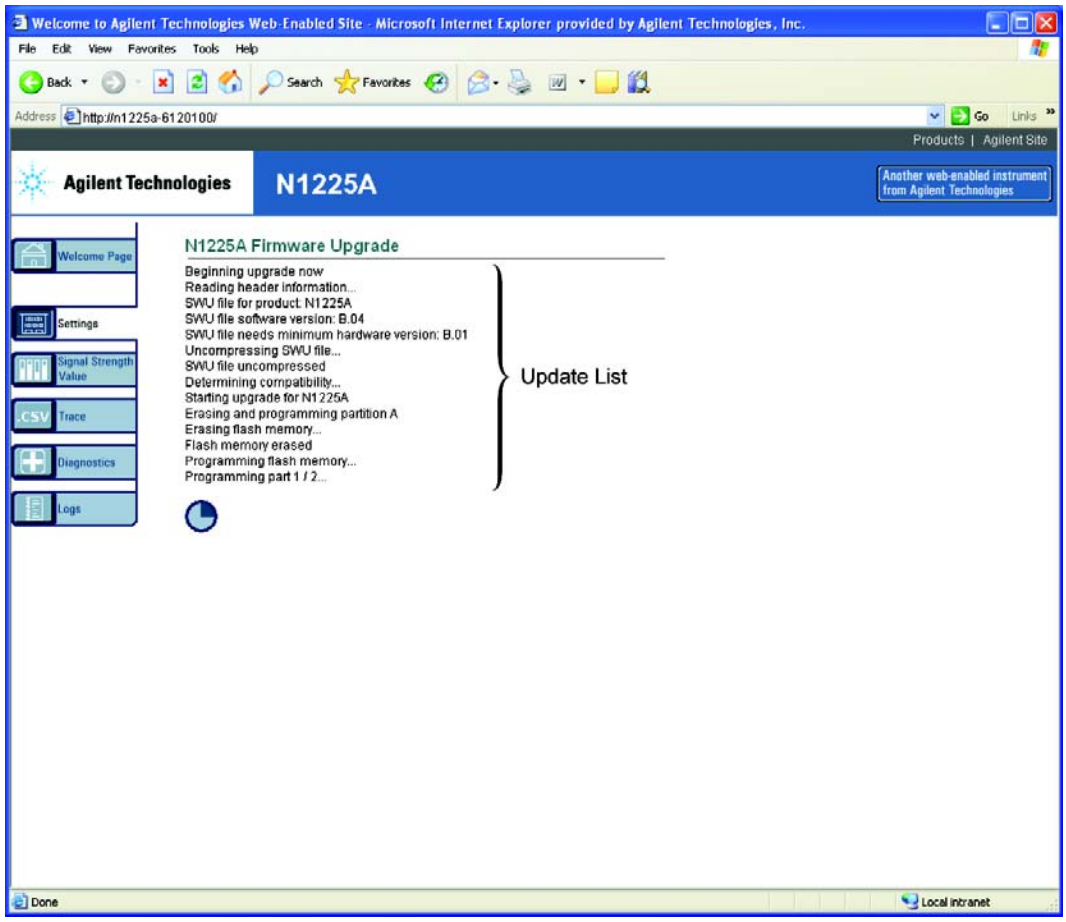


Figure 59 Progress update list

Once the firmware upgrade has completed the "`DONE Upgrade successful`" message is displayed at the end of the progress update list as shown in Figure 60.

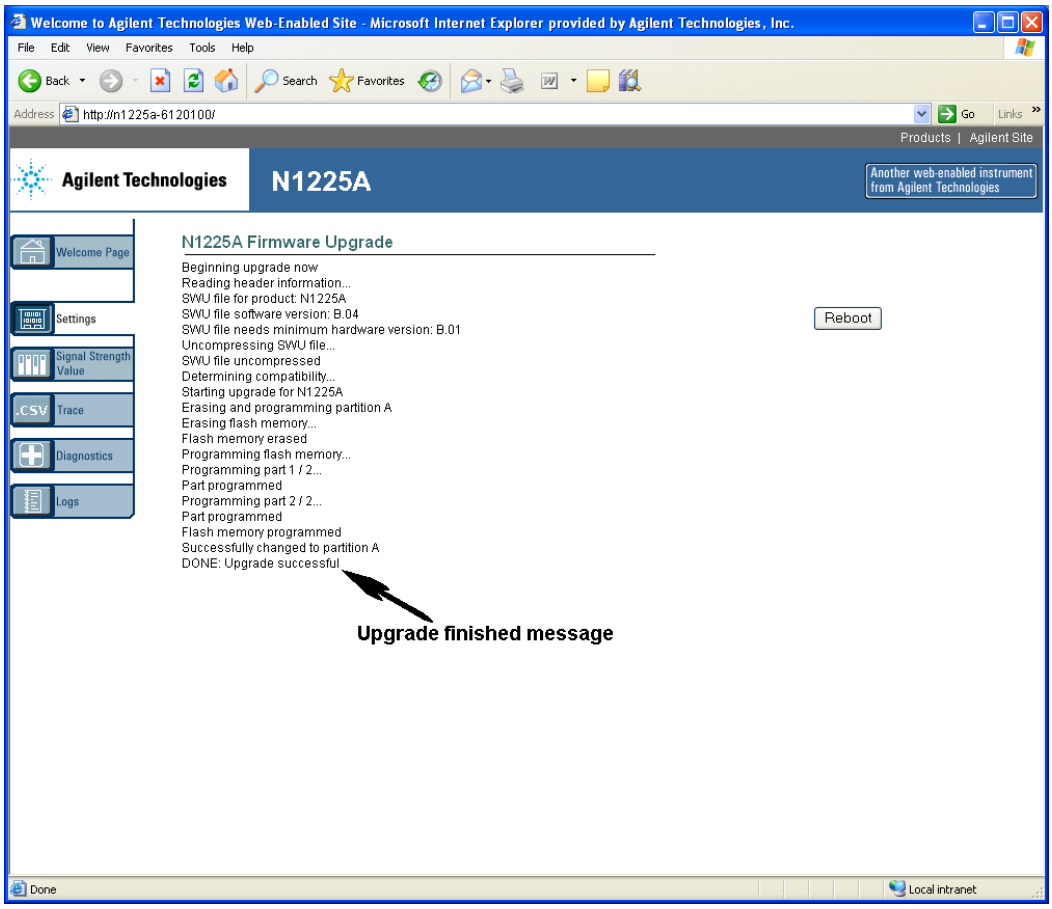


Figure 60 Firmware upgrade finished screen

5 Click on the Reboot button.

The software upgrade is completed.

List of Replaceable Parts

Table 16 lists the replaceable parts.

Table 16 Replaceable Parts

Part	Agilent Part Number
N1225A 4 Channel High Resolution Laser Axis Board for VME, refurbished	N1225-69003
Reference cable	N1225-60203
Front panel	N1225-20201
Injector/ejector handle top	Z4201-60304
Injector/ejector handle bottom	Z4201-60305
ESD gasket	7101-1064
Manual (CDROM)	N1225-13601

Exchange/Rebuilt Assembly

Agilent has an exchange/rebuild N1225A available as Agilent Part Number N1225-69003. The exchange/rebuild assembly consists of all the assembly replaceable parts except the interconnect cables and manual. The old board must be turned in when ordering the exchange/rebuilt assembly.

To obtain replaceable parts, address your order to your nearest Agilent Sales or Service office. Identify parts by Agilent part number.

Warranty

Send the defective unit to your local Agilent Repair Hub, following the instructions you received from the Agilent Call Center.

Non-Warranty

You have the option of ordering the exchange part on-line at *www.parts.agilent.com* or sending the unit to your local Agilent Repair Hub, following the instructions you received from the Agilent Call Center.

8 Specifications

Introduction

This chapter includes information on VME compliance, compatibility with other Agilent VMEbus boards, as well as details on signal output characteristics.

Compatibility with Other Agilent VMEbus Boards

The Agilent N1225A board can replace the Agilent 10897/8 boards in many applications.

Table 17 Slew Rate Comparison (mm / sec)

Type of Optics	Agilent N1225A	Agilent 10897B/C	Agilent 10898A
Linear	4640*	1400	5600
Plane Mirror	2320*	700	2800
High Resolution	1160*	350	1400

* Using a 15 MHz split Laser head.

NOTE Do not bus P2's A and C rows of the 10897A with either the 10898A or the N1225A boards because of low drive capability for the position outputs of the 10897x family of boards.

The N1225A board (as well as the Agilent 10898A, 10895A, 10896A, 10896B and the 10897A boards) complies both electrically and mechanically with Rev C.1 of the VMEbus specification. The two outer rows of the P2 connector are compatible with the 10898A.

CAUTION Inserting the Agilent N1225A board into a slot intended for another board may cause damage.

CAUTION Do not plug an N1225A board into a slot intended for the 10895A board or vice-versa because the functions on the P2 connector are not all the same and damage may result.

CAUTION The N1225A does NOT support hot swap capability.

System Level Specifications

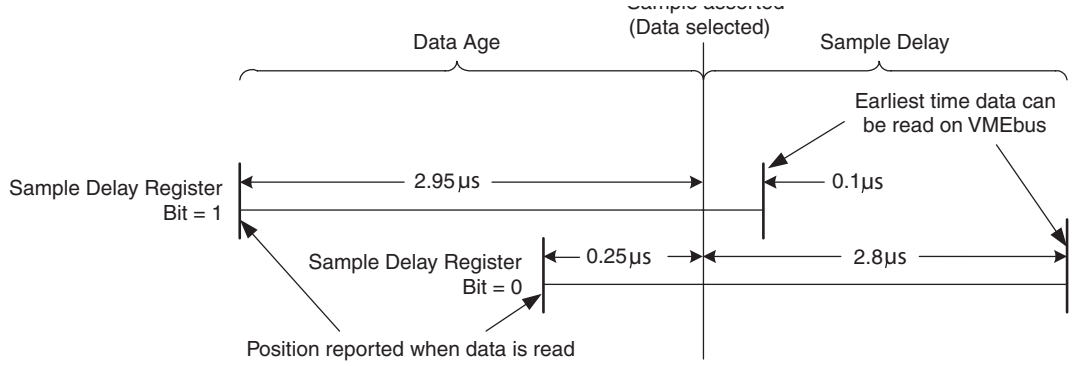
Agilent Technologies N1225A Four-Channel High Resolution Laser Axis Board for VME	
General System Specifications	
Maximum number of boards in system	Eight on reference chain
Measurement resolution	λ/4096 (0.15 nm) with double pass I/F Linear Optics: 0.3 nm
Velocity range (using double pass I/F)	±1.58 m/s with 20 MHz laser head split frequency ±0.87 m/s with 6 MHz laser split frequency ±1.1 m/s with 7.5 MHz laser split frequency ±2.29 m/s with 15 MHz laser split frequency b. Maximum velocity for 20 MHz split is less because of 30 MHz upper limit on receiver.
Maximum axis acceleration	400 g
Working range with plane mirror optics	±10.3 m (37 bits in position register)
Optical Inputs	
Sensitivity	(Estimated power level considered to be measured at input to E1706A connected to 2m long glass fiber) 0.065µW @ 90% ac:dc ratio
Frequency Range	500 kHz to 30 MHz
Maximum input levels:	62.5 µW AC power; 187 µW DC power
Signal Strength Voltage (SSV) update rate (typical, refers to per channel value)	100 Hz
Number of optical channels	Four per board
Number of optical reference inputs	Two maximum for a single board system Three maximum for a two board system
Squelch setting when shipped	Preset to zero (inactive)
Optical input connector	ST Type
Dynamic range	1250:1 maximum (90% ac:dc ratio) 93.5:1 minimum (10% ac:dc ratio)
Reference inputs	One digital reference input
Frequency range	One optical, using channel 4 ST connector 0.5–30 MHz nominal
Reference outputs	One digital reference output
Measure inputs	Four, if reference supplied by another board Three, if one channel is used for reference
Signal Monitoring test points	Front panel scope probe socket for each channel
Status Indication	Signal and error LED for each channel Status LED indicates bootup progress
Fixed data age for P2 data	3.05 µs, typical

Agilent Technologies N1225A Four-Channel High Resolution Laser Axis Board for VME	
Frequency and dynamic range dependent error	<0.6 nm in plane mirror system (estimate)
Velocity resolution	94.3 nm/s
Velocity format	27 bits, 2's complement
Digital Interface	
Position Data Output Rate (over P2 bus)	Maximum 10 MHz/# of axes 36 bit, 2's complement or output 32 contiguous bits out of 37
High Speed Parallel Output	10 bits/axis, 10 MHz simultaneous output 0.768 m/s maximum velocity
N1225A VME characteristics/operations	6U EIA module A16/A24 addressing, GAP D16/D32 data transfer cycles Responds to address modifier codes: $29 Short non-privileged access $2D Short supervisory access $39 Standad non-privileged data access $3D Standard supervisory data access D08(O) Interrupt acknowledge cycles VME 64x (160 pin P1/P2) ANSI/VITA 1-1994 American National Standard for VME64 ANSI/VITA 1-1997 American National Standard for VME64
LAN	10/100 Base T LAN Connection DHCP Enabled Built-in web page server
Power Requirements	
Power requirements	+5 V +0.25 V –0.125 V @ 5.6 A maximum (120 mV_{pp} max. noise below 20 MHz) (80 mV_{pp} max low frequency ripple, below 200 Hz)
Environmental Requirements	
Airflow requirements	400 ft/min, 40 ° C maximum inlet air temperature
Operating environment	The product is intended for use in an industrial or clean room environment
Operating temperature range	0 to 40 ° C
Humidity	10 to 90% RH (non-condensing)
Board Characteristics	
Bootup time	Less than 30 seconds
Data age variation over temperature	+15 ps/° C, estimated
Physical Characteristics	
Weight	0.46 Kg (1 lb)
Packaged Weight	0.77 Kg (1 lb 11 oz)

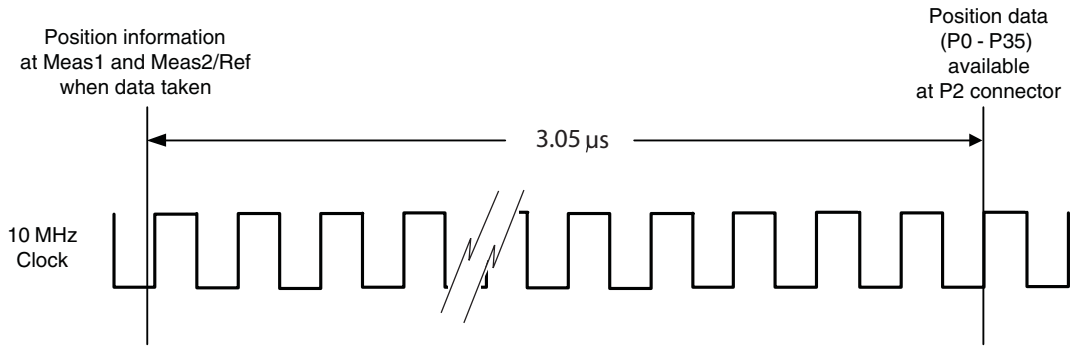
Agilent Technologies N1225A Four-Channel High Resolution Laser Axis Board for VME

P2 Bus Timing

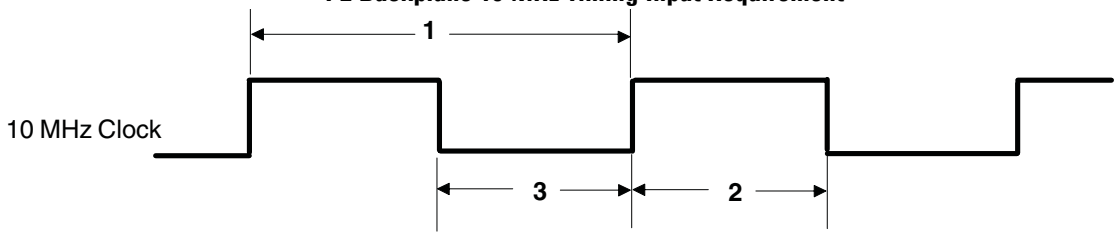
VMEbus Data Age Timing



P2 Data Age Timing



P2 Backplane 10 MHz Timing Input Requirement

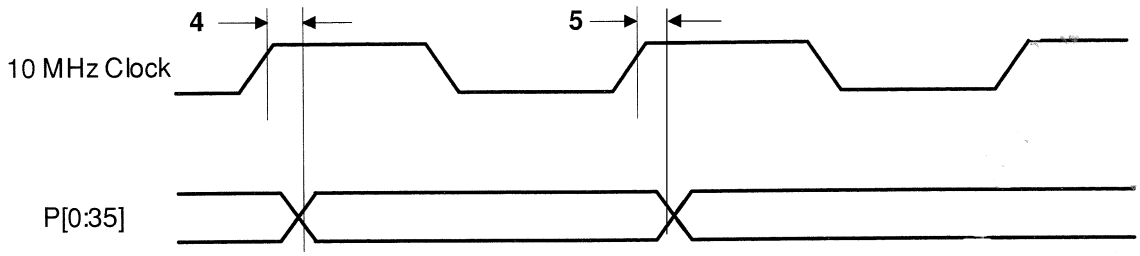


Parameter		Min	Max
1	Clock period	**99.990** ns	**100.010** ns
2	Clock high	45 ns	55 ns
3	Clock low	45 ns	55 ns

Recommended input transition rise/fall rate 10 ns/V
Low-level input voltage = 0.8V (maximum)
High-level input voltage = 2.0V (minimum)
Maximum input voltage = 5.5V

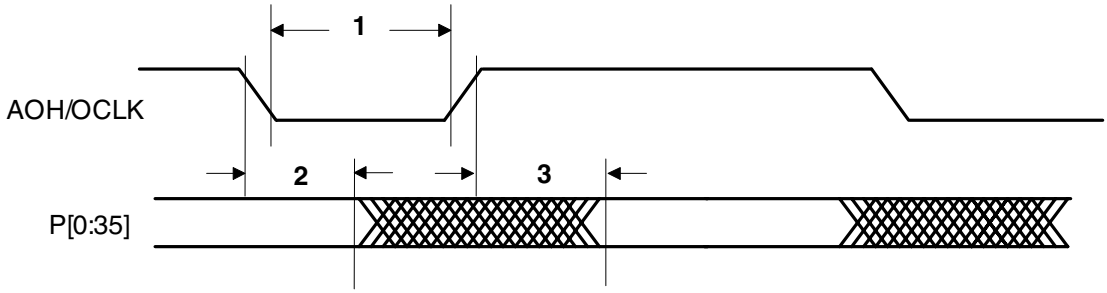
Agilent Technologies N1225A Four-Channel High Resolution Laser Axis Board for VME

P2 Position Output Timing



Parameter		Clock Modes 1 and 3		Clock Mode 2	
		Min	Max	Min	Max
4	Clock to Position Data valid	—	28 ns	—	25 ns
5	Position Data hold time	4 ns	—	2 ns	—

Asynchronous Mode 1 Timing



Parameter		Min	Max
1	AOH/OCLK low	100 ns	—
2	AOH/OCLK low to output invalid	100 ns	—
3	AOH/OCLK high to output valid	—	120 ns

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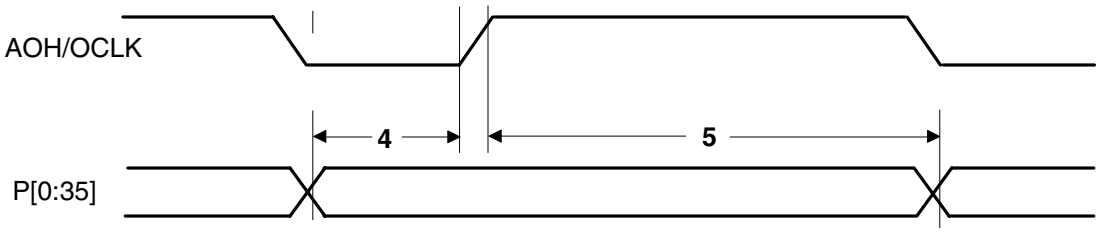
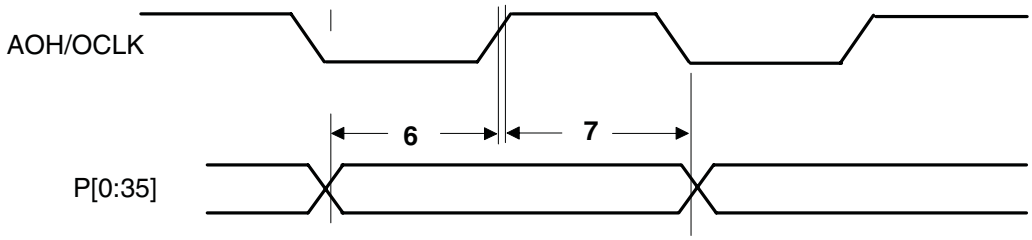
P2 Asynchronous Mode 2 Timing



Parameter		Min	Max
4	Output Data valid to AOH/OCLK high	85 ns	—
5	AOH/OCLK high to Output Data change	**	—

** [(100*N)-20] ns, where N = value loaded in the Output Hold and Rate Control Register.

P2 Asynchronous Mode 3 Timing



Parameter		Min	Max
6	Output Data valid to AOH/OCLK high	35 ns	—
7	AOH/OCLK high to Output Data change	35 ns	—

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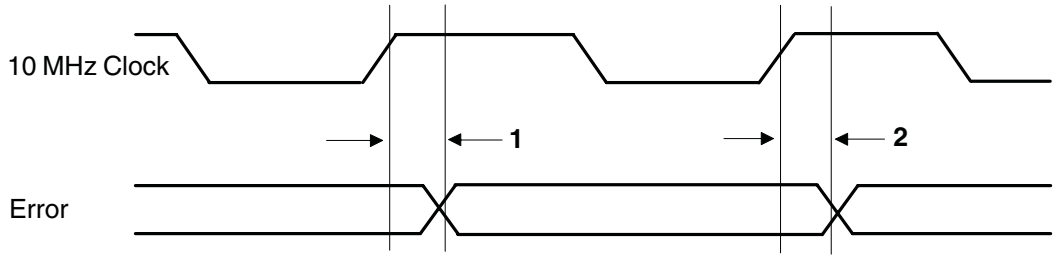
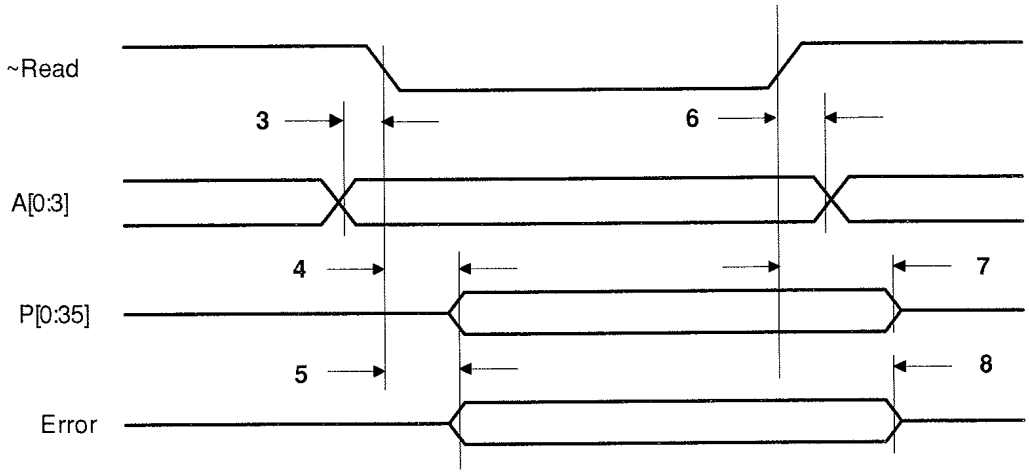
P2 Error Output Timing



Parameter		Min	Max
1	10 MHz Clock to Error output valid	—	65 ns
2	Error output hold from 10 MHz Clock	4 ns	—

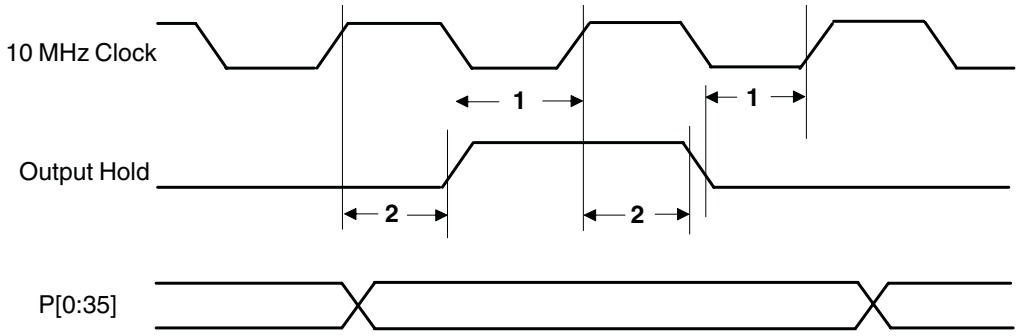
P2 Output Enable Timing



Parameter		Min	Max
3	Address stable to ~Read low	18 ns	—
4	~Read low to Output Data valid	—	27 ns
5	~Read low to Error output valid	—	17 ns
6	Address hold from ~Read	-3 ns	—
7	Output Data hold from ~Read	4 ns	—
8	Error output hold from ~Read	4 ns	—

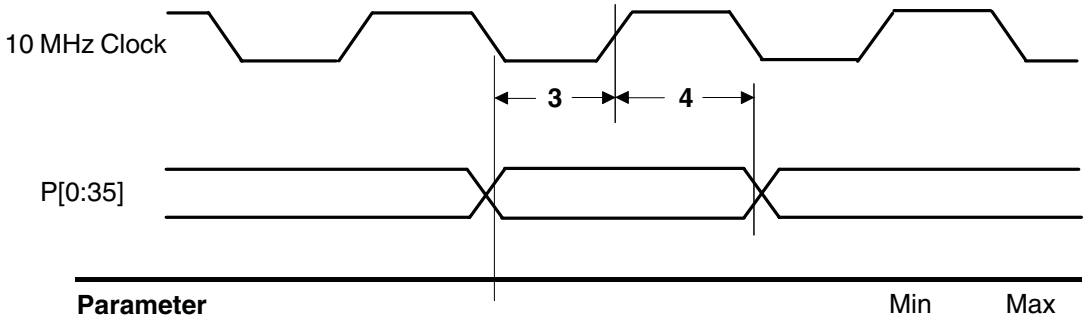
Agilent Technologies N1225A Four-Channel High Resolution Laser Axis Board for VME

P2 Output Hold Timing



Parameter		Min	Max
1	Output Hold to Clock setup time	20 ns	—
2	Output Hold to Clock hold time	0 ns	—

P2 Position Reset Timing



Parameter		Min	Max
3	~ Position Reset to Clock setup time *	20 ns	—
4	~ Position Reset to Clock hold time	0 ns	—

* ~Position Reset may be asynchronous provided it is held active for at least 120 ns.

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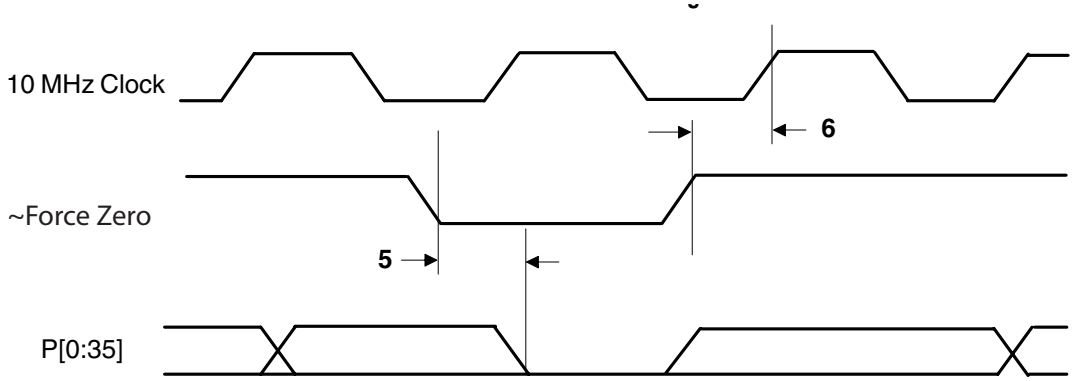
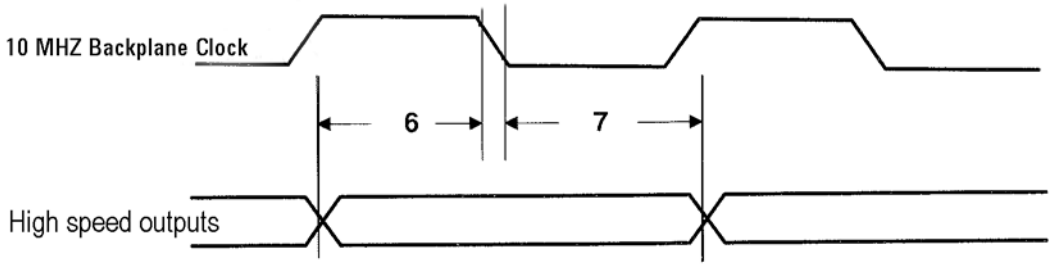
P2 Force Zero Timing



Parameter		Min	Max
5	~Force Zero low to Position Data zero	—	50 ns
6	~Force Zero high to Clock setup time	24 ns	—

P2 High Speed Position Outputs Timing



Parameter		Min	Max
6	Output valid to BP clock high	35 ns	—
7	BP clock high to outputs change	33 ns	—

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Agilent Technologies	**DECLARATION OF CONFORMITY** According to ISO/IEC Guide 22 and CEN/CENELEC EN 45014	CE

Manufacturer's Name: Agilent Technologies, Incorporated
Manufacturer's Address: 5301 Stevens Creek Boulevard
Supplier's Address: Santa Clara, CA 95051
USA

Declares under sole responsibility that the product as originally delivered

Product Name: 4-Channel High-Resolution Laser Avis Board
Model Number: N1225A/P
Product Options: This declaration covers all options of the above products

complies with the essential requirements of the following applicable European Directives, and carries the CE marking accordingly:

The Low Voltage Directive 73/23/EEC, amended by 93/68/EEC
The EMC Directive 89/336/EEC, amended by 93/68/EEC

and conforms with the following product standards:

EMC	Standard	Limit
	IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	
	CISPR 11:1990 / EN 55011:1991	Group 1 Class A
	IEC 61000-4-2: 1995+A1: 1998 / EN 61000-4-2:1995	4 kV CD, 8kV AD
	IEC 61000-4-3: 1995 / EN 61000-4-3: 1995	3 V/m, 80-1000MHz
	IEC 61000-4-4: 1995 / EN 61000-4-4: 1995	0.5 kV signal lines, 1 kV power lines
	IEC 61000-4-5: 1995 / EN 61000-4-5: 1995	0.5 kV line-line, 1kV line-ground
	IEC 61000-4-6: 1995 / EN 61000-4-6: 1995	3 V, 0.15-80 MHz 1 cycle, 100%
	IEC 61000-4-11: 1994 / EN 61000-4-11: 1994	Dips: 30% 10ms; 60% 100ms Interrupt: > 95%@5000ms
	Canada: ICES-001:1998	
	Australia/New Zealand: AS/NZS 2064.1	
	This product was tested in a typical configuration with Agilent Technologies test systems	
Safety	IEC 61010-1:2001 / EN 61010-1:2001	
	IEC 60825-1:1993+A1:1997+A2:2001	
	Canada: CSA C22.2 No. 1010.1:1992	

Supplementary Information:

This DoC applies to above-listed products placed on the EU market after:

1 May 2006
Date

Randall White
Randall White
Product Regulations Manager

For further information, please contact your local Agilent Technologies sales office, agent or distributor, or Agilent Technologies Deutschland GmbH, Herrenberger Straße 130, D 71034 Böblingen, Germany.

Continued from front matter. . .

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Safety Considerations (contd)

WARNING

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Acoustic Noise Emissions

LpA<47 dB at operator position, at normal operation, tested per EN 27779. All data are the results from type test.

Geräuschemission

LpA<47 dB am Arbeits platz, normaler Betrieb, geprüft nach EN 27779.
Die Angagen beruhen auf Ergebnissen von Typenprüfungen.

Electrostatic Discharge Immunity Testing

When the product is tested with 8kV AD, 4kV CD and 4kV ID according to IEC801-2, a system error may occur that may affect measurement data made during these disturbances. After these occurrences, the system self-recovers without user intervention.

Agilent Technologies

Manual Part Number N1225-90012

Printed in U.S.A, JULY 2007